Discontinuous Conduction Mode Operation of the Current-Shaping Modular Multilevel DC–DC Converter

Philippe A. Gray, *Graduate Student Member, IEEE*, and Peter W. Lehn, *Senior Member, IEEE*

***Abstract*— The current-shaping modular multilevel dc–dc converter (CS-MMC) is a recently proposed class of modular multilevel dc–dc converters for dc distribution grid applications consisting of a single string of cascaded voltage-source submodule (VSM) cells, a current-source submodule (CSM), and, notably, no series inductor. In the CS-MMC, since it is the CSM that shapes the string current and there is no series inductor, this frequency can readily be in the medium-frequency range, enabling VSM cells to be realized with low cell capacitance. In the previous work, only continuous conduction mode (CCM) operation of the CS-MMC had been considered, which led to several limitations, including elevated switching losses and low utilization of the semiconductor devices in low output voltage applications. In this work, the discontinuous conduction mode (DCM) operation is proposed for the CS-MMC that addresses these limitations. In traditional dc–dc converters, DCM is determined by the inductor current ripple. However, unique to the CS-MMC, DCM is determined by the VSM capacitor voltage ripple. In this work, the proposed DCM operational approach is presented along with its analysis and control. Both simulation and experimental results from a laboratory-scale converter system are provided for validation.**

***Index Terms*— DC–DC power converters, discontinuous current mode (DCM), medium-voltage dc (MVdc), modular multilevel converter (MMC), soft switching.**

I. Introduction

THE modular multilevel converter (MMC), originally proposed in [2], is an enabling technology for interconnecting ac and dc networks. The MMC features highly desirable properties, including a modular, scalable structure, and the ability to generate multilevel output voltages. Accordingly, the MMC has received significant attention from both academia and industry in recent years. Subsequent to the MMC, other MMC topologies have been proposed for interconnecting ac and dc networks, as in [3]–[5], and for interconnecting dc networks, such as in [6]–[16].

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The authors are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: p.gray@mail.utoronto.ca; lehn@ece.utoronto.ca).

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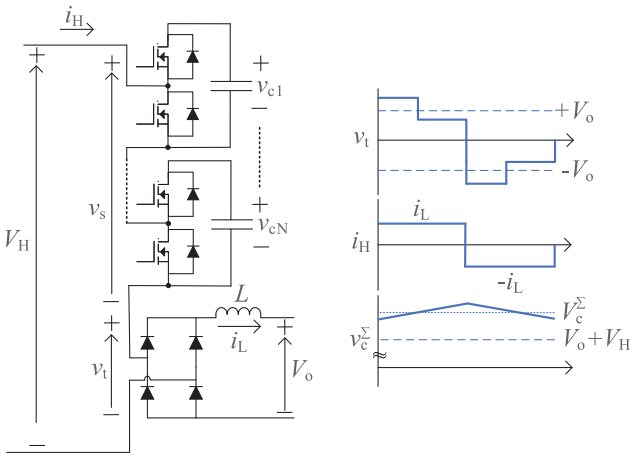


Fig. 1. CS-MMC with CCM operational approach of [11].

Inherently, all the dc–dc topologies for interconnecting dc networks feature some form of internal energy storage. For the front-to-front MMC topologies in [6] and [7], this internal energy is managed similar to that of [2], and therefore, traditional operational approaches developed for the MMC can be employed. In some of the more recent dc–dc topologies, such as the modular multilevel dc–dc converter (M2DC) [8], [9], the HVDC-DC autotransformer (HVDC-AT) [10], and the current-shaping MMC (CS-MMC) [11]–[13], the internal energy transfer mechanism is inherently different from [2], and therefore, these topologies have required novel operational approaches to be developed.

The HVDC-AT and the M2DC topologies of [8]–[10] are suitable for low-to-moderate step ratios and employ parallel strings featuring voltage-source submodules (VSMs) and series inductors. Both topologies circulate ac power internally at a select frequency in hundreds of Hz range to achieve internal energy balance [17]. Conversely, the CS-MMC topology, as shown in Fig. 1, features a single string of VSMs and a current-source submodule (CSM) without a series inductor. The voltages V_H and V_o represent the input and output voltages, respectively. This topology is suitable for high step ratios, and ac power is circulated internally at multiples of the CSM switching frequency that can be in tens of kHz range.

While the CS-MMC topology of [11] is interesting, the operational approach proposed in [11] limits the potential of the topology due to elevated switching losses and low

TABLE I
COMPARING CCM AND DCM OPERATIONS

Parameter	CCM Approach of [11]	Proposed DCM Approach
Total Blocking Voltage of VSM String	$\geq V_H + V_o$	$\approx V_H$
Minimum Number of Switching Operations per Fundamental Period[1]	8 on/8 off	2 on/2 off
• Soft-Switched Operations	8 on	2 on/1 off
• Hard-Switched Operations	8 off	1 off
Constraint on Cell Capacitor Voltage	$V_c < V_o$	None

[1]Each VSM is a half-bridge featuring 2 switches. A switching operation is defined as a switch being turned-on or turned-off.

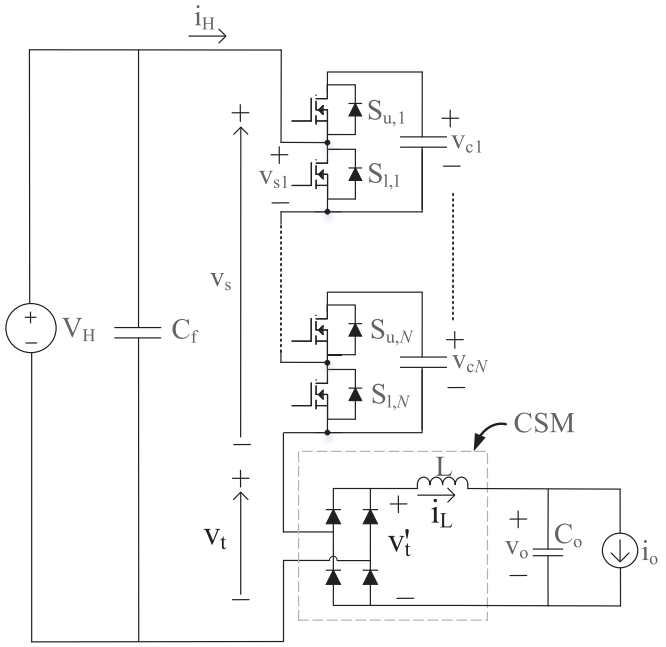


Fig. 2. CS-MMC topology.

utilization of the semiconductor devices in low output voltage applications. To illustrate this, representative operating waveforms are provided in Fig. 1. As can be observed, the voltage v_t, which is generated by switching action of the VSMs, has a four-level voltage waveform, with two-voltage levels on either side of $+V_o$ and $-V_o$. As a consequence, there is a minimum of four switching operations per fundamental period, and the average cell capacitor voltage V_c is implicitly constrained to be less than the output voltage V_o. At the root of these limitations is that, in this operational approach: 1) the VSM string is not able to generate a zero v_t voltage level and 2) active regulation of the cell capacitor voltages is required.

In [18], a control technique for a two-level voltage-source converter (VSC) was proposed termed "type-II inverter control," in which the dc-link voltage is not actively regulated and is instead indirectly set by the reactive power set point of the converter. Consequently, the dc-link voltage will vary depending on the operating point of the converter. By employing this technique, the converter is able to regulate both real and reactive power using only square wave modulation.

Drawing on the concept introduced in [18], this article proposes a new operational approach for the CS-MMC, whereby the cell capacitor voltages are passively regulated with voltage values that are defined by the operating point of the converter. In this approach, the cell capacitor voltage ripple is leveraged to achieve soft turn-off of the VSM string resulting in a discontinuous operating mode (DCM) of operation. This is a unique way of achieving DCM. In traditional dc–dc converters, DCM operation is due to inductor current ripple.

As a consequence of the proposed DCM operational approach, the control for the CS-MMC converter is of much lower complexity, cell capacitor voltages are no longer constrained by the desired output voltage, half of the switching operations are zero-current switched, and the VSM string is only required to generate a two-level voltage waveform. The comparison of the two approaches is summarized in Table I.

A preliminary overview of the DCM operational approach was provided in [1], which included a steady-state analysis. This article expands this work, presenting a dynamic circuit analysis and a complete control logic. In addition, representative experimental results are provided, which validates the soft turn-off mechanism underlying the proposed DCM operational approach.

This article is structured by first providing an overview of the topology. Then, the DCM operating approach is presented. This is followed by a dynamic circuit analysis and a description of the control. Finally, simulation and experimental results from a laboratory-scale converter system are discussed along with conclusions.

II. TOPOLOGY OVERVIEW

The CS-MMC topology is presented in Fig. 2. This represents a more detailed version of the topology presented in Fig. 1. The additions include a low voltage dc load i_o, which is modeled as a current source, and an input and output capacitor, denoted C_f and C_o, respectively, which have been included for filtering purposes. The voltage across the input terminals of the CSM, v_t, is defined by the following expression:

$$v_t(t) = V_H - v_s(t) \tag{1}$$

where $v_s(t)$ is the net VSM string voltage.

If the cell capacitor voltages are well balanced, $v_s(t)$ can be approximated as follows:

$$v_s(t) = \frac{n(t)}{N} v_c^{\Sigma}(t) \tag{2}$$

where N is equal to the total number of VSM cells in the VSM string; $v_c^{\Sigma}(t)$ represents the total sum of VSM cell capacitor

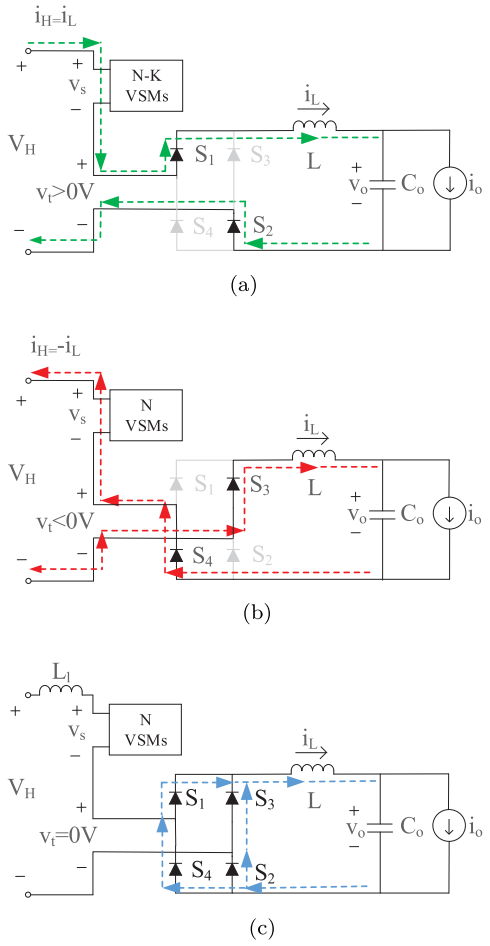


Fig. 3. Operating modes. (a) Charge mode: $v_t > 0$ and $i_H = i_L$. Total duration is $D_1 T_s$. (b) Discharge mode: $v_t < 0$ and $i_H = -i_L$. Total duration is $D_2 T_s$. (c) Freewheeling mode: $v_t = 0$ and $i_H = 0$. Total duration is $(1 - D_1 - D_2)T_s$.

voltages and is calculated as follows:

$$v_c^{\Sigma}(t) = \sum_{k=1}^{N} v_{c,k}(t) \tag{3}$$

and $n(t)$ represents the total number of inserted VSM cells. In reference to Fig. 2, VSM cell 1 is inserted in the circuit when $S_{u,1} = 1$ and $S_{l,1} = 0$ and bypassed when $S_{u,1} = 0$ and $S_{l,1} = 1$.

Equations (1) and (2) show that by varying the number of inserted cells, the voltage applied across the input terminals of the CSM, v_t, can be adjusted. This applied voltage determines the operating mode of the converter.

The converter features three distinct operating modes. The three modes are termed the charge, discharge, and freewheeling modes and correspond to a $v_t > 0$, $v_t < 0$, and $v_t = 0$, respectively. The equivalent circuit for each operating mode is shown in Fig. 3.

Note that the dashed lines in Fig. 3 represent the current paths. In the charge mode, the string current i_H is of positive polarity and equal to the inductor current i_L. In the discharge mode, the string current is of negative polarity and equal to the negative of the inductor current $-i_L$. Both modes represent continuous conduction modes (CCM), since the string current is nonzero.

If the converter enters into the freewheeling mode, as shown in Fig. 3(c), it is operating in DCM. An inductance L_l has been included in Fig. 3(c) to represent the small stray inductance on the input side of the CSM. This stray inductance prevents the string current from instantaneously going to zero at the transition from the discharge to the freewheeling mode.

In the freewheeling mode, the VSM cell capacitors are clamped to the input source v_H. This clamping action leads to the passive voltage balancing of the VSM string and is the fundamental concept underlying the DCM operating approach.

III. Discontinuous Conduction Mode

A. Background

A representative set of operating waveforms for the DCM operational approach is provided in Fig. 4. The total durations of the charge, discharge, and freewheeling modes are $D_1 T_s$, $D_2 T_s$, and $(1 - D_1 - D_2)T_s$, respectively. The term T_s denotes the fundamental period of the string current, D_1 represents a user controllable duty ratio term, and D_2 represents a relative time duration that is dependent on D_1. An expression relating D_2 to D_1 can be obtained by imposing energy balance to the converter.

In this DCM operational approach, internal energy balance is achieved over a fundamental period of the string current. Over each fundamental period, energy balance is achieved if the average power delivered by the input source, P_H, is equal to the average power delivered to the load P_o. Expressions for P_H and P_o can be derived from inspection of Fig. 3 and are as follows:

$$P_H = \overbrace{V_H I_L D_1}^{\text{Charge}} - \overbrace{V_H I_L D_2}^{\text{Discharge}} \tag{4a}$$

$$P_o = I_L V_o. \tag{4b}$$

Note that no power is exchanged with the input source in the freewheeling mode.

By equating (4a) and (4b), the following expression for D_2 in terms of D_1 is obtained:

$$D_2 = D_1 - \frac{V_o}{V_H}. \tag{5}$$

Equation (5) is employed in Section III-B to derive an expression for boundary between continuous conduction mode and discontinuous conduction mode operation.

B. Operating Mode Boundary

If the converter is operating in CCM, only the charge and discharge operating modes occur. This is shown in Fig. 1. Since there is no freewheeling mode in CCM, the boundary between CCM and DCM operations occurs when the freewheeling mode is of zero duration, i.e., $D_2 = D_1'$.

Substituting $D_2 = D_1'$ into (5), the following bound for DCM operation can be established:

$$D_1 < \frac{1}{2} + \frac{1}{2}\frac{V_o}{V_H}. \tag{6}$$

The proposed DCM operational approach requires this constraint to be met.

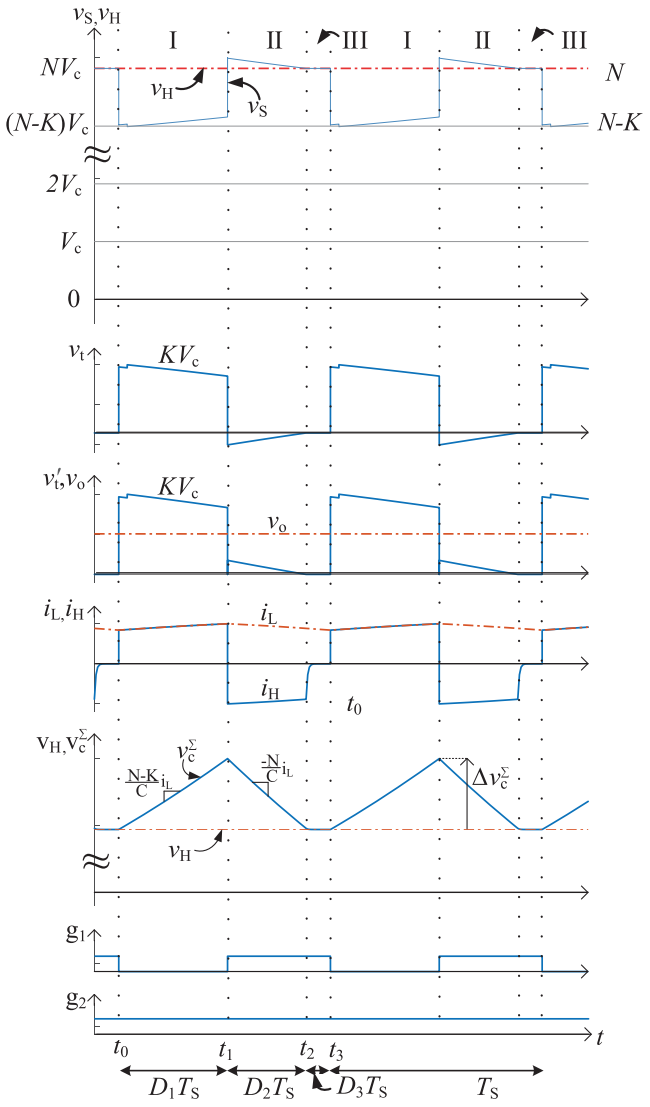


Fig. 4. Representative steady-state operating waveforms. Intervals I–III correspond to the charge, discharge, and freewheeling operating modes, respectively. The number of switched cells $K = 1$. The number of cells $N = 4$.

C. Soft Turn-Off Mechanism

As shown in the representative operating waveforms of Fig. 4, $N - K$ VSM cells are inserted in the charge mode, and N VSM cells are inserted in the discharge and freewheeling modes. The integer variable K corresponds to a number of VSM cells and is selected by the user.[1]

To transition the converter into discharge mode, K VSMs are inserted, and to transition the converter into charge mode, K VSMs are bypassed. The subplot for v_c^Σ in Fig. 4 shows that the VSM cell capacitors charge in the charge mode and discharge in the discharge mode.

No switching actions are required to transition the converter into the freewheeling mode. Instead, this transition is passive and is due to the cell capacitor voltage ripple.

The soft-turn-off of the VSM string occurs at $t = t_2$. At time $t = t_2$, the total sum of cell capacitor voltages v_c^Σ has been discharged to a voltage value of $v_c^\Sigma = v_H$. This starts the turn-off process, causing the string current i_H to rapidly transition from $-i_L$ to 0 A. Since the string current is 0, the next VSM switching actions, occurring at $t = t_3$, represent zero-current switching actions.

Throughout the freewheeling mode, since all N VSM cells are inserted, the total sum of cell capacitor voltages is clamped to the voltage of the input source, i.e., $v_c^\Sigma = v_H$. As a consequence of this clamping, the total sum of cell capacitor voltages is balanced, in a passive manner, as shown in the v_c^Σ subplot.

An expression for the average sum of cell capacitor voltages can be obtained by inspection of Fig. 4. The result is the following:

$$V_c^\Sigma = V_H + \frac{D_1 + D_2}{2} \Delta V_c^\Sigma \tag{7}$$

where ΔV_c^Σ represents the peak-to-peak ripple component, which can also be derived by inspection from Fig. 4, as follows:

$$\Delta V_c^\Sigma = \frac{N - K}{C} i_L D_1 T_s. \tag{8}$$

Equation (7) shows that the average sum of cell capacitor voltages V_c^Σ will vary slightly about V_H based on the size of the ripple.

IV. Operating the Converter

As the CS-MMC does not feature any active switches, it is only through appropriate gating of the VSMs that the control objectives of the CS-MMC are achieved. The conversion ratio for the converter is defined by the following expression[2]:

$$\frac{V_o}{V_H} = D_1 \frac{K}{N} \tag{9}$$

where D_1 is subject to the DCM constraint of (6). If (9) is substituted into (6), the DCM constraint can be reformulated in terms of a constraint on K as follows:

$$K > \frac{2NV_o}{V_H + V_o}. \tag{10}$$

This constraint ensures that the converter operates in DCM. For low output voltages, a minimum value of $K = 1$ is selected. For higher output voltages, a value of $K > 1$ is selected. This article considers K to be a fixed value.

As per (9), by adjusting the duty ratio D_1, the output voltage V_o of the converter is controlled.

Only two unique gating signals need to be generated to control the converter. The gating signals are denoted g_1 and g_2 in Fig. 4 and are mathematically expressed as follows:

$$g_1 = \begin{cases} 0, & 0 < t < D_1 T_s \\ 1, & D_1 T_s < t < T_s \end{cases} \tag{11a}$$

$$g_2 = 1 \quad \forall t \tag{11b}$$

where g_1 and g_2 are distributed to a total of K and $N - K$ VSM cells each, respectively. The result is the net VSM string

[1] To select K, please refer to (10).

[2] Equation (9) can be derived by applying volt–second balance to the CSM inductor L. The relevant volt–second equations are provided later in (14b) for the charge mode, (17b) for the discharge mode, and (18b) for the freewheeling mode.

voltage waveform of v_s in Fig. 4. Note that a VSM cell is inserted when the gating signal is 1 and bypassed when the value is 0.

As noted earlier, the total sum of cell capacitor voltages is balanced over each fundamental period; however, the individual VSM cell capacitors are not necessarily balanced. To address this, the VSM cells are sorted based on their relative states of charge.

V. Circuit Analysis

To inform the control for the converter, dynamic state equations are derived in this section for the charge, discharge, and freewheeling modes.

A. Charge Mode

The charge mode is presented in Fig. 3(a). In this mode, the voltage at the input terminals of the CSM is as follows:

$$v_t(t) = -\left(\frac{N-K}{N}\right) v_c^{\Sigma} + V_{\mathrm{H}}. \tag{12}$$

The voltage $v_t(t)$ is positive since, at the beginning of each fundamental period (i.e., at $t = t_0$ and t_3), the total sum of cell capacitor voltages is given by

$$v_c^{\Sigma}(0) = V_H. \tag{13}$$

The positive voltage forward biases the diodes S_1 and S_2, leading to a string current of $i_H = i_L$. Note that the inductor current i_L will always be positive ($i_L > 0$) due to the orientation of the CSM diode bridge. Since the string current is positive, the dc input source delivers power to the VSM string and the CSM. The time derivative of the inductor current and the total sum of cell capacitor voltages v_{c}^{Σ} during this mode can be calculated as follows:

$$C\frac{dv_{\mathrm{c}}^{\Sigma}}{dt} = (N-K)i_{\mathrm{L}} \tag{14a}$$

$$L\frac{di_{\mathrm{L}}}{dt} = -\left(\frac{N-K}{N}\right) v_{\mathrm{c}}^{\Sigma} + V_{\mathrm{H}} - v_o \tag{14b}$$

where C is the capacitance of one VSM cell capacitor; L is the inductance of the CSM inductor.

Since, at the beginning of the charge mode, $v_c^{\Sigma}(0) = V_H$, v_c^{Σ} at the end of the charge mode can be expressed as follows:

$$v_c^{\Sigma}(D_1 T_s) = V_{\mathrm{H}} + \Delta V_{\mathrm{c}}^{\Sigma}. \tag{15}$$

Note that the initial condition of v_c^{Σ} in the discharge mode is $v_c^{\Sigma}(D_1 T_s)$. Since i_{L} is a positive value, $v_c^{\Sigma}(D_1 T_s) > V_H$.

B. Discharge Mode

While $N - K$ cells are inserted in the circuit for the charge mode, N cells are inserted for the discharge mode. Therefore, K additional cells are inserted. In the discharge mode, as shown in Fig. 3(b), the voltage at the input terminals of the CSM is given by

$$v_t(t) = -v_{\mathrm{c}}^{\Sigma}(t) + V_H. \tag{16}$$

At the beginning of the discharge mode, since $v_c^{\Sigma}(D_1 T_s) > V_H$, it follows that $v_t(t)$ in (16) is negative. This negative voltage forward biases the diodes S_3 and S_4 leading to a string current $i_H = -i_L$. Due to the negative string current, it is now the VSM string that delivers power in this mode, and consequently, the inserted VSMs are discharged. Power is delivered from the VSM string to the dc input source and the CSM. The time derivative of the inductor current and the total sum of cell capacitor voltages v_{c}^{Σ} is calculated as follows:

$$C\frac{dv_{\mathrm{c}}^{\Sigma}}{dt} = -Ni_{\mathrm{L}} \tag{17a}$$

$$L\frac{di_{\mathrm{L}}}{dt} = v_{\mathrm{c}}^{\Sigma} - V_{\mathrm{H}} - v_o. \tag{17b}$$

During the discharge mode, the total sum of cell capacitor voltages v_c^{Σ} decreases. Once v_c^{Σ} decreases to the value of V_H, the voltage across the input terminals of the CSM, v_t, is zero.

C. Freewheeling Mode

The freewheeling mode is presented in Fig. 3(c). In this mode, all four diodes of the CSM conduct current. The path of the CSM inductor current is graphically shown in Fig. 3(c). Since all four diodes are conducting, independent current loops are formed on either side of the CSM. Due to the independent current loops, in this mode, the string current i_H varies independently of the CSM inductor current i_L.

In the representative operating waveforms of Fig. 4, the string current is shown to damp out to zero during the freewheeling mode. When the string current is zero, the time derivative of the CSM inductor current and the total sum of cell capacitor voltages are given by

$$C\frac{dv_{\mathrm{c}}^{\Sigma}}{dt} = 0 \tag{18a}$$

$$L\frac{di_{\mathrm{L}}}{dt} = -v_o. \tag{18b}$$

Since N cells are inserted in the freewheeling mode, and $N - K$ cells are inserted in the charge mode, K cells are bypassed to transition the converter into the charge mode. Since the string current is equal to zero at the end of the freewheeling mode, these switching operations are zero-current switched.

VI. Dynamic-State Analysis

In this section, small-signal linearized equations for the CSM inductor current i_{L}, the output voltage v_o, and total sum of cell capacitor voltages v_{c}^{Σ} are derived. This derivation follows in a similar manner to that developed in [19] for dc–dc converters operated in DCM.

The small-signal ac equations for i_{L} and v_o can be obtained by applying volt–second balance to inductor L and charge balance to capacitor C_o. By using the expressions derived in (14), (17), and (18) and neglecting nonfirst-order ac terms, the following are derived:

$$L\frac{d\hat{i}_L}{dt} = \hat{d}_1\frac{V_H K}{N} - \hat{v}_o \tag{19a}$$

$$C_o\frac{d\hat{v}_o}{dt} = \hat{i}_L - \hat{i}_o \tag{19b}$$

where $\hat{(\cdot)}$ designates a small-signal quantity.

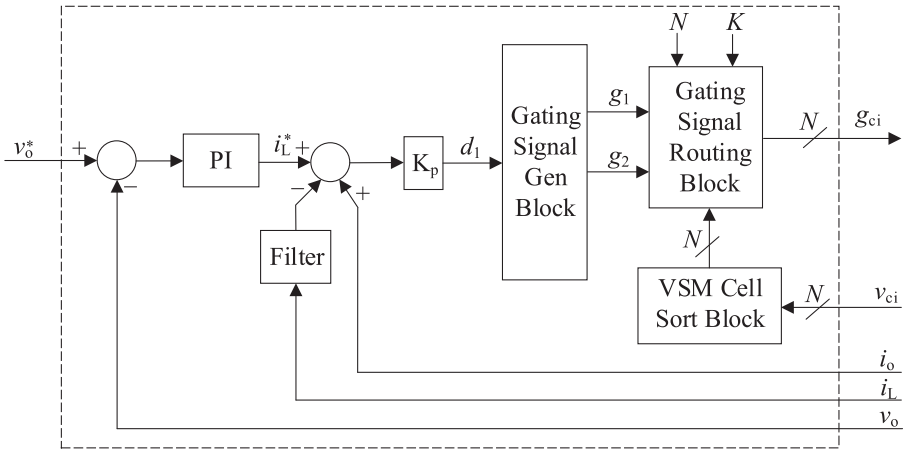


Fig. 5. Complete control logic including inner current control, outer voltage control, and capacitor balancing.

Due to the DCM operation of this converter, the small-signal ac equation for v_c^{Σ} can be stated as follows:

$$\frac{C}{N}\frac{d\hat{v}_c^{\Sigma}}{dt} = 0. \tag{20}$$

The result of (20) is consistent with the findings of [19].

An expression for the small-signal term $\hat{v}_c^{\Sigma}$ as a function of $\hat{i}_L$ and $\hat{d}_1$ can be obtained by inspection of Fig. 4, resulting in the following:

$$\hat{v}_c^{\Sigma} = \frac{2N-K}{2N}\frac{N-K}{C}D_1T_s(D_1\hat{i}_L + 2I_L\hat{d}_1). \tag{21}$$

The controller proposed in Section VII is based on the small-signal linearized ac equations of (19) and (20).

VII. Control Design

The controller proposed for implementing the proposed DCM operational approach is provided in Fig. 5. The measured inputs to the controller are v_o, i_L, i_o, and the individual cell capacitor voltages $v_{c,i}$ for all $i \in [1, N]$. The outputs of the controller are the gating signals to the individual VSMs, g_{ci}, where g_{ci} corresponds to the gating signal to VSM i. The blocks denoted "PI," and "K_p" denote a proportional integral control and proportional control, respectively.

The controller regulates the output voltage v_o to the reference value v_o^* by adjusting the time varying duty cycle d_1 whose steady-state value is D_1. Based on d_1, the gating signal g_1 is generated. The g_1 and g_2 functions were defined earlier in (11).

As can be seen, the total sum of cell capacitor voltages is not regulated in this controller since the total sum of cell capacitor voltages is balanced naturally. However, a sort-and-select technique is employed to ensure that the individual cell capacitor voltages are balanced with respect to each other. In this sort-and-select technique, the gating signals g_1 and g_2 are distributed to the N VSM cells depending on their relative state of charge. More specifically, the gating signal g_1 is distributed to the K cells of greatest states of charge; the gating signal g_2 is distributed to the $N-K$ cells of the lowest states of charge.

TABLE II
Comparing CCM and DCM for a 3750–380-V Application

Parameter	CCM Approach of [11]	DCM Approach: Design 1	DCM Approach: Design 2
Blocking Voltage	4500	3760	3760
Number of Switching Operations per Fundamental Period	8 on/8 off	4 on/4 off	4 on/4 off
• Soft-Switched	8 on	4 on/2 off	4 on/2 off
• Hard-Switched	8 off	2 off	2 off
Cell Voltage, V_c	375	376	752
Number of VSMs, N	12	10	5

VIII. Simulation Results

In this section, the steady-state and transient simulation results are presented for the CS-MMC topology. One envisioned application for the CS-MMC is to interface a future dc household to a dc distribution grid. Accordingly, the simulations are of a 3.75-kV_{dc} converter rated for 5.7 kW of power with an output voltage of 380 V. This represents a step-down ratio of 9.9:1. The fundamental frequency of the string current is $f_{ac} = 5$ kHz, where $f_{ac} = 1/T_s$.

For this specific 3.75-kV–380-V application, the CCM- and DCM-based operational approaches are compared in Table II. Table II presents the main circuit parameters for three separate designs, the first design is based on the CCM approach of [11], and the second and third designs are based on the proposed DCM approach and referred to as DCM design 1 and DCM design 2, respectively. In addition, a simulated loss comparison for the three designs is provided in Appendix C.

In both DCM designs 1 and 2, the number of switched cells is equal to 2, i.e., $K = 2$, to provide an unbiased

TABLE III
MAIN CIRCUIT PARAMETERS FOR SIMULATION AND EXPERIMENTAL RESULTS

Parameter	Sim.	Exp.	Unit
Rated Input Voltage, V_H	3750	500	V
Rated Output Voltage, V_o	380	51	V
Rated Power, P_r	5.7	0.72	kW
Fundamental Freq., f_{ac}	5	5	kHz
Cell Voltage, V_c	752	104	V
Number of VSMs, N	5	5	-
VSM Capacitor, C	40	40	μF
CSM Inductor, L	5	5	mH
Output Capacitor, C_o	200	2500	μF
Cells Switched, K	2	2	-

loss comparison. In both the CCM design and the DCM design 1, the average cell capacitor voltage is maintained to a voltage value of $V_c \approx 375$ V. From Table II, the DCM design 1 is shown to be advantageous compared with the CCM design as it features both a lower VSM count and a reduced number of hard-switched operations.

While the DCM design 1 shows advantages over the CCM design, as highlighted in Table I, one of the primary advantages of the DCM approach is that the cell capacitor voltage is not constrained by the output voltage V_o. Therefore, in DCM design 2, the VSM count is reduced from ten to five VSM cells. For a five-VSM-cell design, the average cell capacitor voltage is $V_c = 752$ V. Due to the reduced VSM string conduction losses expected in DCM design 2, it is DCM design 2 that is considered in this article.

The detailed main circuit parameters for the simulation and experimental results are provided in Table III.

A. Steady-State Simulation Results

The steady-state simulation results are provided in Fig. 6. For these results, an output voltage of $v_o = 380$ V and a load of 5.7 kW have been considered. The waveforms provided are similar to those of Fig. 4 but with additional plots for all five VSM cell capacitor voltages, $v_{c,1}$–$v_{c,5}$, as well as zoomed-in plots for i_L and v_o.

As can be observed, the output voltage v_o is well regulated to the reference value of 380 V. The total sum of cell capacitor voltages v_c^{Σ} is observed to return to an initial value of 3750 V, which is equal to the dc input source voltage V_H, before the end of each fundamental period. This implies that v_c^{Σ} is balanced. The five capacitor voltages $v_{c,1}$–$v_{c,5}$ are also shown to be balanced.

The first fundamental period occurs from $t = 0$ to 0.2 ms. By inspection of the individual cell capacitor voltages over that first fundamental period, it can be inferred that the gating signal g_1 is being distributed to VSM 3 and VSM 5 and g_2 to VSMs 1, 2, and 4. Over this fundamental period, the cell capacitor voltages of VSMs 1, 2, and 4 increase, and the cell capacitor voltages of VSMs 3 and 5 decrease.

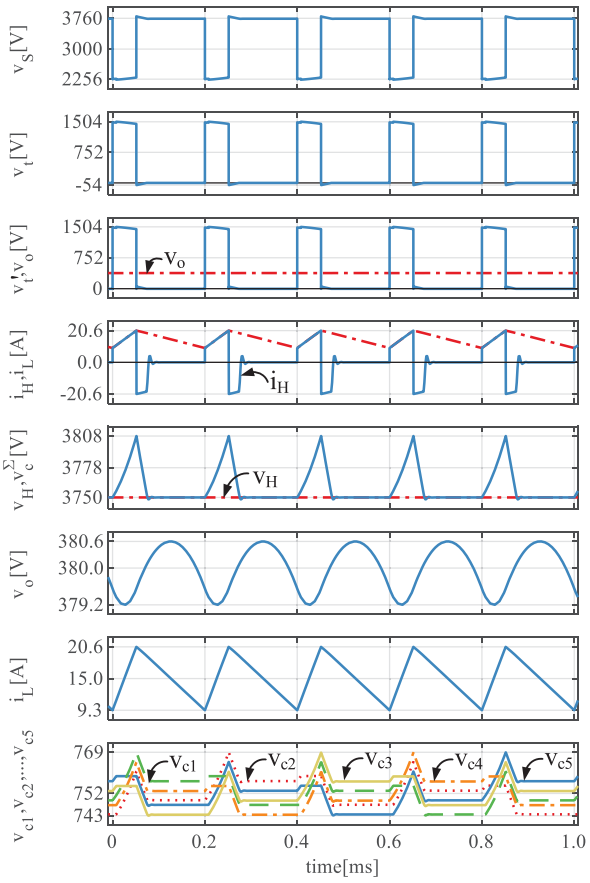


Fig. 6. Steady-state simulation results.

The total sum of cell capacitor voltages v_c^{Σ} has an average value of 3760 V. Consequently, the average cell capacitor voltage is 752 V, which is similar to that predicted by (7). This average cell capacitor voltage will vary slightly based on the converter operating point. The CSM inductor current is shown to be 15 A with a peak current ripple of 5.6 A. The string current i_H takes on values of i_L, $-i_L$, and 0 A in each fundamental period, which indicates that all three operating modes (charge, discharge, freewheeling) are realized. It can also be observed that when the string current i_H reaches 0 A, there is no change to the total sum of VSM cell capacitor voltages, as expected.

B. Transient Simulation Results

To verify the dynamic performance of the converter, a step change in the load i_o and the output voltage reference v_o^* are imposed. The results are provided in Fig. 7. Compared with the steady-state results of Fig. 6, only two of the VSM cell capacitor voltage waveforms are shown, and an additional waveform has been provided for the duty ratio term d_1.

A step change in the load from 1 to 5.7 kW occurs at $t = 1$ ms. The system settles within 6 ms. In response to the step change, the duty ratio d_1 increases from its steady-state value of D_1. When $d_1 > D_1$, the power delivered to the input terminals of the CSM is greater than the power delivered to the load. Conversely, when $d_1 < D_1$, the power delivered to

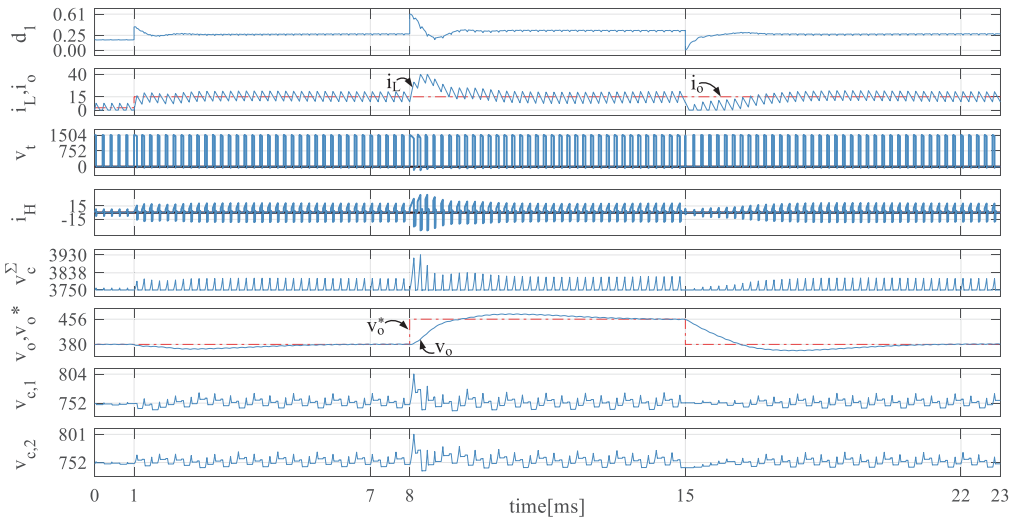


Fig. 7. Transient simulation results.

the input terminals of the CSM is less than the power delivered to the load.

In response to the load change, d_1 nearly instantaneously increases to a maximum value of $d_1 = 0.39$. This duty ratio value is greater than the steady-state value of D_1, and therefore, the power being delivered to the input terminals of the CSM exceeds the power being delivered to the load. The net difference in power results in a net increase in power being delivered to the CSM inductor. As a consequence, the CSM inductor current i_L increases. As the inductor current cannot instantly change, there is a duration of time when the inductor current is less than the load current, i.e., $i_L < i_o$. During this time, a deficit of power is delivered to the output, resulting in a decrease in output voltage v_o. When the inductor current is greater than the load current, i.e., $i_L > i_o$, an excess of power is delivered to the output resulting in an increase in the output voltage v_o. Therefore, the inductor current and the output voltage are coupled, as observed in Fig. 7.

A step change in the output voltage reference v_o^* from 380 to 1.2*380 V is imposed at $t = 8$ ms and from 1.2*380 to 380 V at $t = 15$ ms. In both cases, the system settles within approximately 7 ms. In response to the step change to 1.2*380 V, d_1 increases to a maximum value of 0.61, which causes the inductor current i_L to transiently increase to a value above the load current i_o. This difference in the two currents causes v_o to rise to the new reference value of $1.2 * 380$ V. Conversely, in the response to the step change to 380 V, d_1 decreases to a minimum value of 0 causing v_o to decrease to the reference.

From the v_c^Σ waveform, it can be observed that v_c^Σ returns to $V_H = 3750$ V before the end of each fundamental period.

IX. Experimental Results

In this section, the experimental results obtained from the laboratory-scale converter system are described. A picture of the experimental setup is provided in Fig. 8. The steady-state experimental results are provided in Fig. 9. The transient

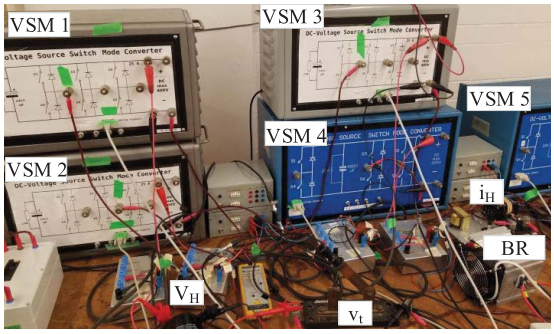


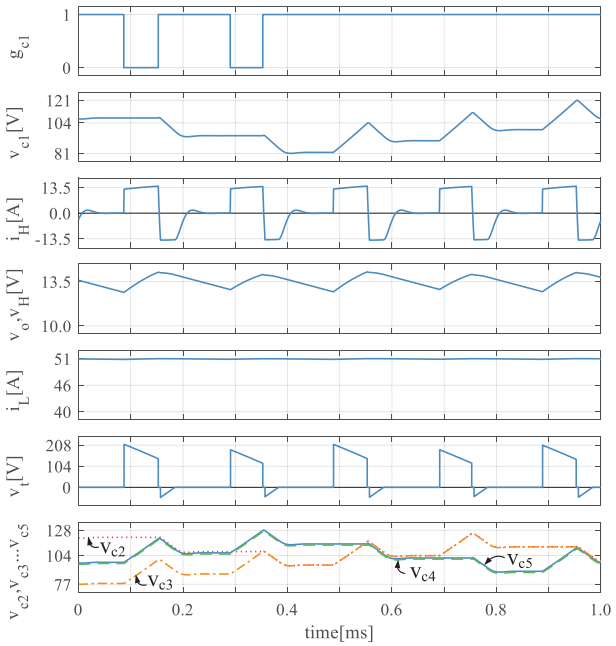
Fig. 8. Experimental setup. BR denotes the bridge rectifier.

experimental results are provided in Figs. 10 and 11. Simulation results based on the experimental system parameters are provided in Figs. 9(a), 10(a), and 11(a), which validates the experimental findings. The input source voltage is 500 V_{dc}, and the output voltage is variable from 51 to $1.2 * 51$ V. The maximum load considered is 720 W. The number of switched cells is $K = 2$, and the average VSM cell capacitor voltage is 104 V. The cells are sorted every second fundamental period.

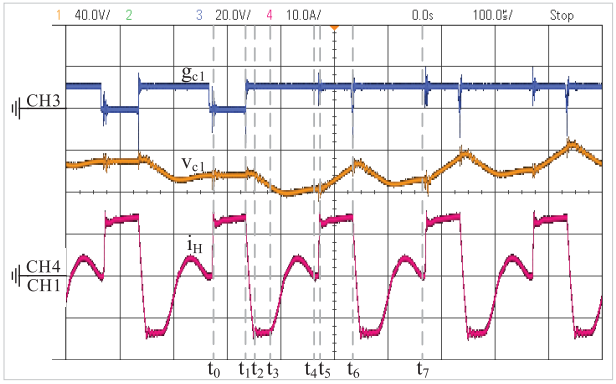
A. Steady-State Experimental Results

For the steady-state results shown in Fig. 9, an output voltage of 51 V and a load current of 13.5 A_{dc} are considered. A total of five periods are captured in Fig. 9. Note that the interval from $t = t_0$ to t_5 represents one fundamental period. The following waveforms are provided in Fig. 9(b): the gating signal to VSM cell 1, g_{c1}, the VSM 1 cell capacitor voltage v_{c1}, and the string current i_H. In Fig. 9(c), additional waveforms are provided for the input source voltage v_H, the inductor current i_L, the output voltage v_o, and the voltage across the input terminals of the CSM v_t.

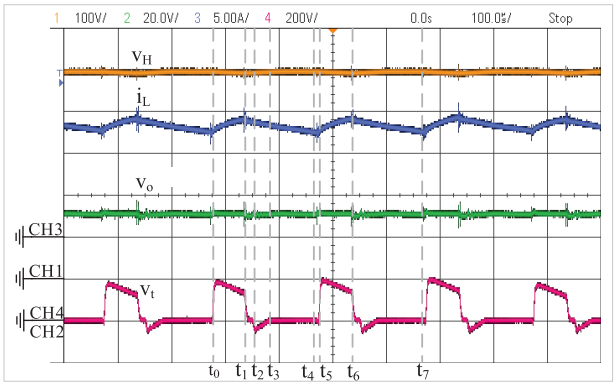
In the charge mode, three VSM cells are inserted. This imposes a voltage across the input terminals of the CSM equivalent to two cell capacitor voltages, as shown in Fig. 9(c).



(a)

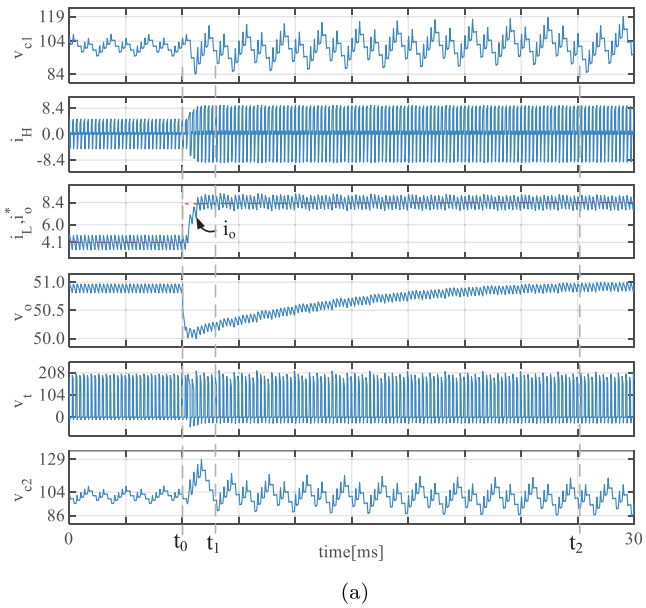


(b)

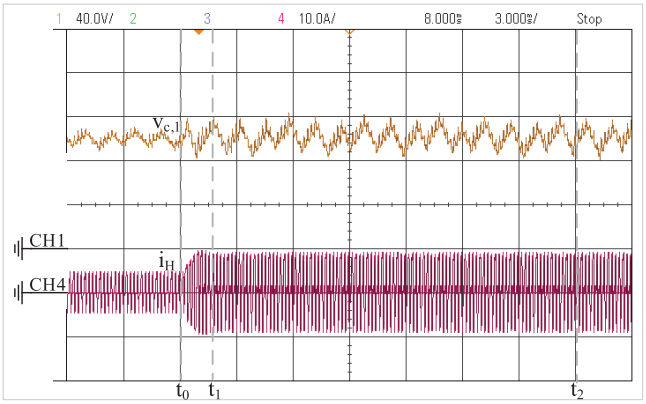


(c)

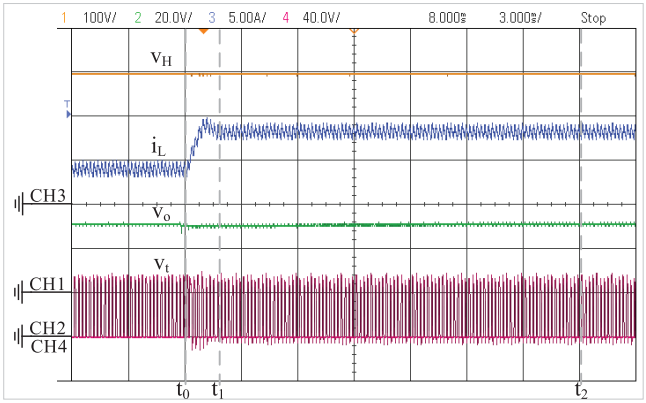
Fig. 9. Experimental steady-state results: 500/51 V and $I_o = 13.5$ A. (a) Simulation results for validation. (b) Experimental results. CH1 $= v_{c,1}$, CH3 $= g_{c,1}$, and CH4 $= i_H$. (c) Experimental results. CH1 $= v_H$, CH2 $= v_o$, CH3 $= i_L$, and CH4 $= v_t$.



(a)



(b)



(c)

Fig. 10. Experimental transient results: step change in load I_o from 4.1 to 8.4 A_{dc}. (a) Simulation results for validation. (b) Experimental results. CH1 $= v_{c,1}$ and CH4 $= i_H$. (c) Experimental results. CH1 $= v_H$, CH2 $= v_o$, and CH3 $= i_L$.

For the discharge and freewheeling modes, five VSM cells are inserted, and the voltage across the input terminals of the CSM, v_t, is near 0. Due to the ripple voltage on the VSM cells, the voltage v_t is less than 0 during the discharge operating mode. It is this ripple voltage on the VSM cells that forward biases the diode bridge causing the converter to transition into the discharge mode and the string current i_H to reverse polarity.

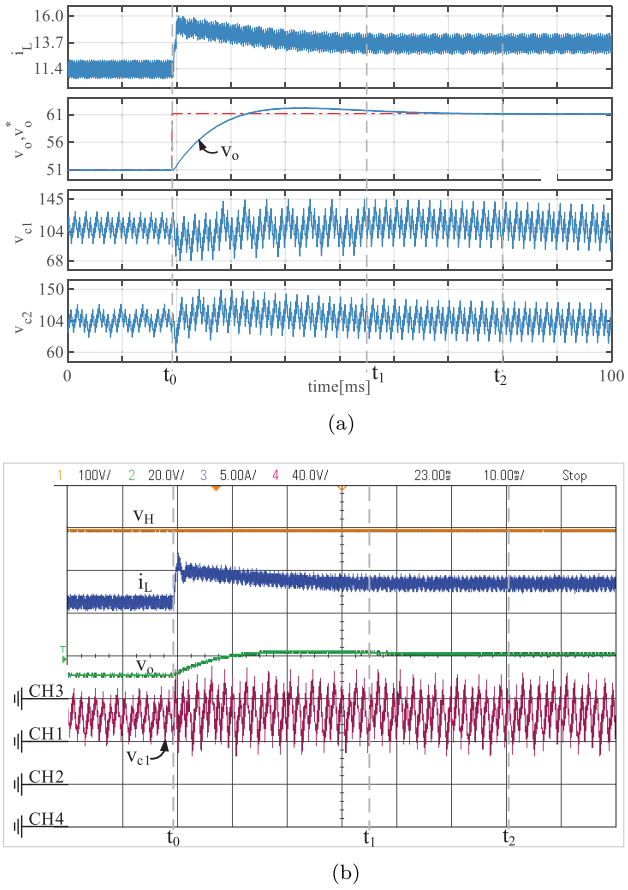


Fig. 11. Experimental transient results: 20% step change in output voltage reference V_o^* from 51 to 61 V_{dc}. (a) Simulation results for validation. (b) Experimental results. CH1 = v_H, CH2 = v_o, CH3 = i_L, and CH4 = $v_{c,1}$.

It can be observed that the output voltage v_o is well regulated. The charge, discharge, and freewheeling modes can also be observed to start at $t = t_0$, t_2, and t_3, respectively. During the freewheeling mode interval, the amplitude of the string current i_H is not equal to the CSM inductor current i_L and the string current damps out to 0 over that interval. The two VSM cells that are bypassed to transition the converter from freewheeling-to-charge mode are, therefore, zero-current switched. This transition occurs at t_0 and at t_5, for instance.

When g_{c1} is "ON," the VSM cell 1 is inserted in the circuit, and conversely, when g_{c1} is "OFF," the VSM cell 1 is bypassed. During the charge mode, when VSM cell 1 is inserted, the VSM cell 1 capacitor voltage is seen to increase, and conversely, when the VSM is bypassed, the capacitor voltage does not change. All cells are inserted during the discharge mode. In this mode, the VSM 1 cell capacitor voltage is seen to decrease.

As the freewheeling operating mode occurs in each fundamental period, passive regulation of the total sum of cell capacitor voltages is achieved.

B. Transient Experimental Results

In the transient results shown in Fig. 10, a step change in the load from 4.1 to 8.4 A occurs at $t = t_0$. It takes approximately 1.5 ms for the inductor current i_L to reach a steady-state. The cell capacitor voltage ripple increases by a factor of approximately 2, as expected, due to the enlarged current pulses. The capacitor voltage can also be observed to be well regulated to a value of ≈104 V throughout the transient. The output voltage undergoes a small transient voltage sag after the step change in load similar to a conventional buck converter.

In the transient results shown in Fig. 11, a step change in the output voltage reference from 51 to $1.2 * 51$ V occurs. It takes approximately 60 ms for the system to reach a steady-state. Since the load is a resistor in this experimental system, the inductor current increases proportionally from 11.4 to 13.7 A as the output voltage v_o increases from 51 to 61 V. The capacitor voltage is shown to be 104 V with a voltage ripple component that increases with the inductor current.

X. Conclusion

This article proposes a novel operating approach for the CS-MMC converter based on a DCM of operation. A unique feature of the CS-MMC is that DCM is determined by the VSM cell capacitor voltage ripple. In DCM, the VSM cell capacitors are clamped to the input source voltage V_H. This feature is exploited in the proposed DCM operational approach to achieve passive voltage balancing of the VSM string.

This work shows that when the CS-MMC is employed for low output voltage applications, DCM operation is advantageous over CCM operation. Due to the passive voltage balancing of the VSM string, the controller is of lower complexity, and the number of switching operations is significantly reduced, half of which are zero-current switched.

In addition, by operating in DCM, a lower VSM cell count can be achieved since the $V_c < V_o$ constraint of [11] is eliminated together with the reduced VSM string blocking voltage requirement.

Appendix

In this section, expressions are derived for the total number of cells N and the average switching frequency f_{sw}. In addition, a simulated loss analysis is presented.

A. Selecting the Total Number of Cells

The number of VSM cells N should be selected based on the maximum value of the total sum of cell capacitor voltages v_c^Σ, as given by (15). Accordingly, the number of cells N can be chosen by the following formula:

$$N = \left\lceil \frac{V_H + \Delta V_c^\Sigma}{V_{VSM}} \right\rceil \tag{22}$$

where $\lceil \cdot \rceil$ represents the ceiling function, and V_{VSM} is the maximum allowable VSM cell capacitor voltage as constrained by the VSM switch voltage rating. Recall that an expression for ΔV_c^Σ was derived earlier in (8).

B. Average Switching Frequency

To determine the average switching frequency, it is first necessary to determine the number of switching operations per

TABLE IV
COMPONENTS CONSIDERED FOR LOSS STUDY

Parameter	CCM Approach of [11]	DCM Approach: Design 1	DCM Approach: Design 2
VSM MOSFETs	Cree C3M0015065D		Cree C3M0016120D
CSM Diode	Cree C4D40120D		
Inductor, L	Vacuumschmelze 6128-X230		

fundamental period. The number of VSM switching operations can be broken down as follows.

1) *Charge-to-Discharge Mode:* K cells are inserted. This corresponds to K switches being turned-on and K switches being turned off.
2) *Freewheeling-to-Charge Mode:* K cells are bypassed. Similarly, this corresponds to K switches being turned-on and K switches being turned off.

Therefore, there are a total of 2k turn-on and 2k turn-off switching operations per fundamental period. Since the total number of switches is equal to $2N$, the average switching frequency f_{sw} can be calculated as follows:

$$f_{\text{sw}} = \frac{K}{N} f_{\text{ac}}. \tag{23}$$

C. Comparing Losses of DCM and CCM Approaches

This section provides a simulated loss comparison for the DCM- and CCM-based operational approaches. The losses are evaluated at the nominal operating point of 3750–380 V and 5.7 kW for the three designs detailed in Table II. For this loss comparison study, only switch conduction losses, switching losses, and magnetic losses are considered, which was similarly done in [20]. The losses are simulated with PLECS in the manner described by [21] based on SiC semiconductors that are the envisioned switch type for this application. This was the approach in [22]. The components considered for the loss study are provided in Table IV, and the results are presented in Fig. 12.

The total losses for the CCM design, DCM design 1, and DCM design 2 are calculated to be 84.0, 72.7, and 46.8 W, respectively. Therefore, both DCM-based designs feature reduced conversion losses compared with the CCM-based design. In this study, the fundamental frequency of the string current is limited to 5 kHz to be consistent with the laboratory-scale converter system. As a consequence, the VSM switching losses are low relative to the VSM conduction losses.

In both the CCM design and the DCM design 1, the cell capacitor voltages are maintained to a similar voltage value of ≈375 V. The total switching loss of the VSM string for DCM design 1 is calculated to be 0.8 W. This represents a 58% reduction in switching losses compared with the 1.9 W of switching losses for the CCM design. This is expected due to the reduced number of hard-switching operations in the DCM-based approach.

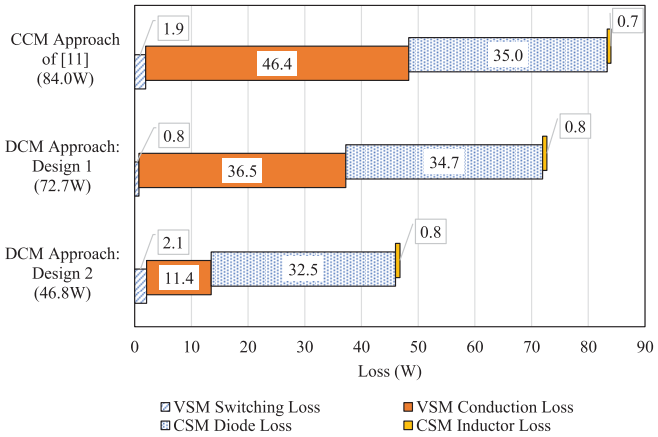


Fig. 12. Loss comparison. Total losses for CCM approach, DCM Design 1, and DCM Design 2. The simulated operating point is 3750–380 V with 5.7 kW of power and a fundamental ac frequency of 5 kHz.

Comparing the VSM conduction losses across the three designs shows that the DCM design 2 offers the lowest VSM string conduction losses. This is a consequence of the reduced VSM cell count and the extended duration of the freewheeling mode. Recall that in the freewheeling mode, the string current rapidly transitions to 0 A; at that point, there are no further VSM string conduction losses until the next fundamental period.

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Philippe A. Gray (Graduate Student Member, IEEE) received the B.A.Sc. degree (Hons.) in engineering science and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2010 and 2013, respectively, where he is currently pursuing the Ph.D. degree.

From 2012 to 2013, he was a Visiting Researcher with ABB Corporate Research, Västerås, Sweden. From 2014 to 2017, he was a System Design Engineer of high-voltage dc (HVdc) transmission systems with General Electric (GE), Stafford, U.K. His current research interests include technologies for medium-voltage dc (MVdc) and HVdc applications, multilevel converters, and grid integration of distributed resources.

Peter W. Lehn (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Manitoba, Winnipeg, MN, Canada, in 1990 and 1992, respectively, and the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 1999.

In 1999, he joined the Faculty of the University of Toronto. In 2001, he was a Visiting Professor with the University of Erlangen–Nuremberg, Erlangen, Germany. His current research interests include HVdc technologies, grid integration of storage and renewables, power electronics for electric vehicles, and theoretical analysis of power electronic systems.

Dr. Lehn has served as an Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION from 2013 to 2019.