Common-Mode Current Prediction in a Non-isolated Onboard EV Fast Charger

Amirhossein Nazeri[1]
Department of Electrical and Computer Engineering
University of Toronto
Toronto, Canada
a.nazeri@mail.utoronto.ca

Chatumal Perera[1]
Department of Electrical and Computer Engineering
University of Toronto
Toronto, Canada
chatumal.perera@utoronto.ca

Peter W. Lehn
Department of Electrical and Computer Engineering
University of Toronto
Toronto, Canada
lehn@ece.utoronto.ca

2024 IEEE Applied Power Electronics Conference and Exposition (APEC) | 979-8-3503-1664-3/24/$31.00 ©2024 IEEE | DOI: 10.1109/APEC48139.2024.10509239

***Abstract*—Integrated chargers eliminate the need for a dedicated onboard charger by repurposing drivetrain components for charging, thereby reducing the cost and weight of an EV. The dual inverter drive (DID)-based integrated charger further improves efficiency by eliminating the isolation stage. However, the lack of isolation leads to higher common-mode (CM) currents, which poses a challenge in complying with the strict safety standards associated with EV charging. This challenge can be overcome using an appropriate modulation scheme and the proper design of a CM filter. This paper presents a comprehensive analytical model that accurately predicts and analyzes these CM currents, providing a full understanding of their quantitative and qualitative nature. Additionally, an extensive experimental validation of the model is presented, offering practical insights for the development of DID-based integrated chargers.**

Keywords—Common-mode current, Electric vehicle, Non-isolated charger, Fast charging station, Integrated onboard charger, Dual inverter drive

I. Introduction

As concerns regarding climate change grow, electric propulsion is moving to substitute internal combustion engine [1]-[3]. Electric vehicles (EVs) have garnered widespread interest among countries attempting to reach their climate change commitments [4,5]. One of the most prominent impediments to wider adoption of EVs on roadways is the long time required for charging. This barrier must be overcome by the installation of fast charging stations (FCSs) [6].

The DC fast charging concept is broadly defined in IEC and SAE standards under mode 4 and DC level 2, respectively. Following SAE J1772, DC FCSs can deliver power up to 400 kW to the EV battery energy storage system [7,8]. Such high power enables automotive engineers to design FCSs to lower the charging duration. However, maximizing efficiency and minimizing cost are two main challenges with regard to this endeavor. Since traditional FCSs incorporate a galvanic isolation transformer, they introduce relatively high costs, and reduced power densities and efficiencies at high power levels [9]. Thus, the significance of non-isolated FCSs becomes apparent to overcome these limitations [10].

Integrated EV chargers [11]-[14] repurpose the existing drivetrain components for charging, eliminating the need for a dedicated onboard charger. This lowers the component count of an EV, reducing cost and weight. The dual inverter drive (DID) can be used as an integrated charger [14]-[16], as shown in Fig. 1. During driving operation, two 3-phase inverters, each accompanied by its battery pack, are used to drive an open-ended winding motor. In DC fast charging mode, the positive DC terminal of the top inverter and the negative DC terminal of the bottom inverter are connected to a DC source, thereby completing the charging current path. The two inverters regulate the current drawn from the DC source (DC bus or DC grid), charging the battery packs while the motor zero-sequence inductance acts as a harmonic filter.

Several standards have been established to regulate safety requirements for EV chargers. In North America, the UL 2231 standard discusses protective requirements for on/off board and (non-)isolated EV chargers, including devices for ground monitoring, charging circuit interrupting, and isolation monitoring [17,18]. However, the absence of isolation in an FCS introduces a minor challenge to comply with the safety standards, resulting from higher common-mode (CM) currents. The CM current labeled as i_{CM} in a non-isolated DC FCS is shown in Fig. 2, resulting from parasitic current paths.

Considering the voltage level of more than 400 V utilized by DC FCSs, UL 2231 requires the use of a charging circuit interrupting device (CCID) with a trip level of 20 Measurement Indication Units (MIU) at the electric vehicle supply equipment

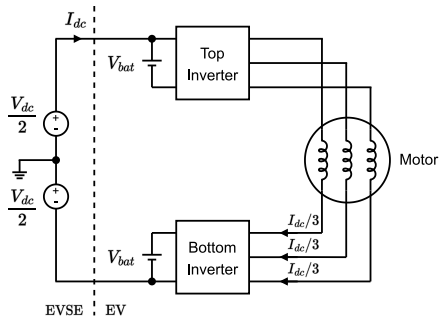


Fig. 1. DID-based DC integrated charger.

[1] Both authors contributed equally to this work.

This research was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) under Grant CRDPJ 513206-17.

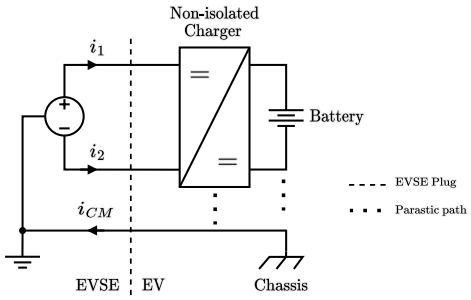


Fig. 2. CM current in a non-isolated integrated EV DC charger.

(EVSE) end [18]. The CCID is a specialized safety device which detects ground faults by effectively measuring the CM current (i_{CM}) and interrupts the charging process. Thus, it protects users from potential electrical hazards at both the charging station and vehicle. For non-isolated chargers, this presents a challenge in complying with safety trip limits due to CM currents. Avoiding nuisance tripping events is critical, which can be overcome by using an appropriate modulation scheme and suitable design of a CM filter. However, such design requires a comprehensive understanding of the nature of CM currents. Predicting these currents is extremely difficult due to their parasitic nature. Moreover, there is limited literature regarding the CM currents in the DID-based integrated charger of Fig. 1. A CM current analysis for the AC charging version of the integrated charger in Fig. 1 is provided in [19] but focuses more on the modulation strategy.

The contribution of this paper can be viewed to be three-fold. Firstly, a comprehensive analytical model capable of providing an accurate prediction of the quantitative as well as the qualitative nature of these currents is presented. Secondly, a method of explicitly measuring CM impedances, which is critical for achieving accurate predictions is described. Lastly, beyond theoretical analysis, the remainder of this paper discusses the experimental validation of this model, which provides valuable practical insights into the design of non-isolated DC FCSs.

II. Defenitions

A. Differential-mode and Common-mode Quantities:

In general, circuit operation can be divided into two modes: Differential Mode (DM) and CM. DM refers to the expected functioning of a circuit as outlined in its schematic, while CM is an undesirable mode that can occur due to the existing asymmetries and parasitic components in a circuit. The DM and CM voltage and current are defined at a set of terminals shown in Fig. 3. Definitions are given in (1)-(4), where the node voltages are defined with respect to an arbitrary reference, P [20].

$$V_{DM} \triangleq v_{1P} - v_{2P} \tag{1}$$

$$V_{CM} \triangleq \frac{1}{2}(v_{1P} + v_{2P}) \tag{2}$$

$$i_{DM} \triangleq \frac{1}{2}(i_1 - i_2) \tag{3}$$

$$i_{CM} \triangleq i_1 + i_2 \tag{4}$$

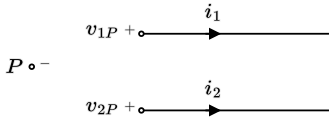


Fig. 3. Diagram of CM and DM definitions.

B. Measurement Indication Unit:

The MIU is a unit for touch current that provides a measurement indicating the physiological effects when electric current flows through the human body. These effects include both perception and startle-reaction, that cause electrical sensation and involuntary muscular contraction, respectively. Figure 4 and Table 1 represent the touch current networks simulating the impedance of the human body. Effectively, the touch current measurement circuit functions as a lowpass filter that attenuates high-frequency components of the CM current labeled as i_{CM}. Equation (5) presents the touch current in MIU.

$$i_{MIU} = \frac{V_{out}\,[\text{mV}]}{500\,[\Omega]} \tag{5}$$

TABLE I. Touch Current Network Parameters

Parameter	Symbol	Value
human skin resistance	R_S	1.5 kΩ
human skin capacitance	C_S	220 nF
Human body internal resistance	R_B	500 Ω
Resistance of frequency sensitive sub-network	R_1	10 kΩ
Capacitance of frequency sensitive sub-network	C_1	22 nF

III. CM Current Derivation in DID-based DC charger

The layout of the DID-based DC integrated charger is illustrated in Fig. 5. The EVSE comprises a centrally grounded DC source with three output terminals. Three cables connect the EVSE to the vehicle: the positive cable to the top inverter's positive DC terminal (P), the negative cable to the bottom inverter's negative DC terminal (N), and the earth cable to the vehicle's chassis ground (E). The CM current flowing through the system i_{CM} is defined to be the sum of the positive and negative cable currents i_p and i_n , as in Fig. 5. Z_{line} refers to the combined effective impedance due to the positive, negative and earth cables from the source to the EVSE, which is explained in detail in Section IV. Z_{src} refers to impedance of the source while Z_{chg} refers to the combined impedance of the cables (Z_{line}) and the charger as seen from the source output (Fig. 5).

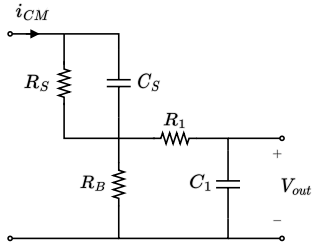


Fig. 4. Touch current measurement circuit as defined in [17].

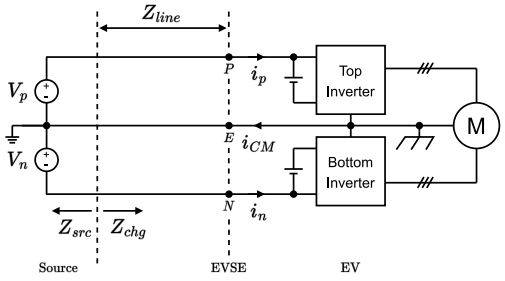


Fig. 5. Layout of the system.

A. CM Equivalent Circuit

Due to the parasitic capacitive coupling between some of the components in the charger with the grounded chassis, there exist paths for CM current to flow. Figure 6 represents the parasitic elements of the system that contribute to the CM currents' flow, including the inverter Y-capacitances C_y and the motor winding capacitances C_w. In addition, the system includes leakage inductance resulting from the motor windings (L_{ls}) as well as impedances due to the charging cables (Z_{line}) and source (Z_{src}).

For the purpose of CM current analysis, the circuit in Fig. 6 may be simplified into the equivalent circuit shown in Fig. 7 using the CM definitions described in Section II. The CM circuit model consists of a single voltage source v_{CM} driving the current i_{CM}. v_{CM} is the CM of the six phase voltages of the dual inverters measured with respect to the midpoint of the DC link of each inverter and can be expressed as in (6).

$$v_{CM} = \frac{v_{a1} + v_{b1} + v_{c1} + v_{a2} + v_{b2} + v_{c2}}{6} \tag{6}$$

The impedances in this model are the CM impedances resulting from the source, cables, inverter Y- capacitances and motor winding parasitic elements. It is important to note that these CM impedances are not necessarily equal to the equivalent parallel or series impedance of individual parasitic elements. For instance, $Z_{line,CM}$ is not simplistically equal to $Z_{line}/2$. This is due to the distributed nature of these impedances and potential mutual couplings between individual elements, impacting only the CM component of voltage and current. Therefore, the best way to estimate these CM impedances is to measure them directly wherever possible.

B. Analytical Model

The CM current of the DID-based integrated DC charger can be calculated analytically using the transfer function (7) derived from the CM circuit model in Fig. 7.

$$I_{CM}(s) = \frac{1}{Z_{chg,CM}(s) + Z_{src,CM}} \cdot \left(\frac{Z_{y,CM}(s)}{Z_{y,CM}(s) + Z_{w,CM}(s)} \right) \cdot V_{CM}(s) \tag{7}$$

where,

$$Z_{chg,CM}(s) = Z_{line,CM}(s) + Z_{y,CM}(s) \parallel Z_{w,CM}(s) = Z_{line,CM}(s) + \frac{Z_{y,CM}(s) \cdot Z_{w,CM}(s)}{Z_{y,CM}(s) + Z_{w,CM}(s)} \tag{8}$$

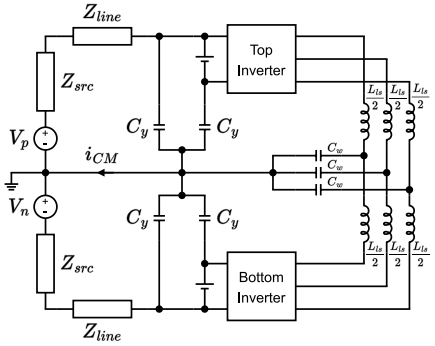


Fig. 6. Parasitic model of the system.

$Z_{chg,CM}$ is the equivalent CM impedance due to the charger and the charging cables as seen from the charging station (see Fig. 5, 7). This impedance term is defined explicitly since it will be used frequently in the remainder of this paper. The right-hand side of (7) can be understood to be the product of an admittance term, a voltage divider gain term and a voltage term. Hence it can be rewritten as

$$I_{CM}(s) = \frac{1}{Z_{eq,CM}(s)} \cdot G_{vd}(s) \cdot V_{CM}(s) \tag{9}$$

where,

$$Z_{eq,CM}(s) = Z_{chg,CM}(s) + Z_{src,CM}(s) \tag{10}$$

$$G_{vd}(s) = \frac{Z_{y,CM}(s)}{Z_{y,CM}(s) + Z_{w,CM}(s)} \tag{11}$$

$Z_{eq,CM}$ is the impedance seen by the CM current. The voltage divider gain term $G_{vd}(s)$ gives the fraction of V_{CM} dropped across $Z_{y,CM}$. Hence, the voltage $G_{vd}(s) \cdot V_{CM}(s)$ is the actual voltage driving the CM currents that is also apparent from Fig. 7. The impedance terms in the above equations can be measured in the manner stated in Section IV. And, for best results, the measured impedance curves shown in Fig. 10 should be used rather than lumped passive elements to represent the impedances.

It is beneficial to express v_{CM} in terms of its distinct frequency components. For a DID-based DC integrated charger implementing both vertically and horizontally interleaved switching, the expression for v_{CM} can be derived as in (12). Horizontal interleaving is achieved by phase shifting the carriers of the phases by 120º. Vertical interleaving between inverters is achieved by using the same carriers for both inverters, but complementary duty cycle references.

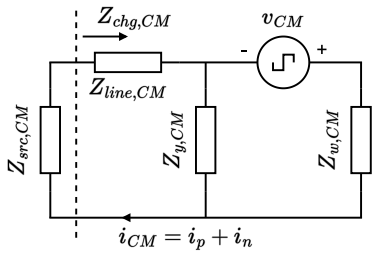


Fig. 7. CM equivalent circuit model for the system.

$$v_{CM}(t) = \sum_{n=1}^{\infty} \frac{2V_{bat}}{3\pi(2n\text{-}1)} \cdot \sin(3\pi(2n\text{-}1)D) \cdot \cos(2\pi \cdot 3(2n\text{-}1)f_{sw}t) \quad (12)$$

Where, the duty ratio D is related to the ratio between the DC grid voltage V_{DCgrid} and V_{bat} through the relation in (13).

$$D = \frac{V_{DCgrid}}{2 \cdot V_{bat}} \quad (13)$$

Thus, v_{CM} can be expressed as an infinite sum of sinusoidal signal components. The frequencies of these sinusoids are always odd triplen multiples of the switching frequency f_{sw} while the amplitudes of the sinusoids are dependent on the battery pack voltage V_{bat} and the duty ratio D at which the inverters are operated. This expression is derived assuming that the battery pack voltages of the two inverters are equal. As indicated by (12), all harmonic amplitudes are zero if $D = \{0, \frac{1}{3}, \frac{2}{3}, 1\}$, meaning v_{CM} is also zero and consequently so too i_{CM}. Conversely, all harmonic amplitudes peak at $D = \{\frac{1}{6}, \frac{1}{2}, \frac{5}{6}\}$, maximizing the CM voltage v_{CM}. The variation of harmonic voltage component amplitudes with duty ratio for a constant V_{bat} at f_{sw}=10 kHz is illustrated in Fig. 8. It is worth mentioning that the number of harmonic amplitude zeros and peaks increase with the harmonic order. Given the reasonable assumption that V_{DCgrid} remains relatively constant during charging, the only dynamic variable influencing i_{cm} in (7)-(13) is V_{bat}. This implies that the charging current level has no impact on the CM currents. The variation of the CM voltage harmonics with V_{bat} at V_{DCgrid} =200 V is shown in Fig. 9. The plot implies that v_{CM} and consequently i_{CM} is largest when V_{bat}=V_{DCgrid} and smallest (zero) when V_{bat}= 0.75V_{DCgrid}. These correspond to duty ratio values of 1/2 and 2/3, respectively.

IV. Definition and Measurement of CM Impedances

This section discusses the definition of the CM impedances in Fig. 7.

$Z_{src,CM}$: This is the total effective CM impedance due to the DC source seen from the DC bus at the charging station. The measurement of this impedance requires the disconnection of the charger and its associated charging cables from the DC bus. Subsequently, a short circuit should be established between the positive and negative buses, followed by the measurement of the impedance between the earth bus and these shorted buses. It is worth noting that this measurement can pose practical challenges. To avoid this issue in the experimental setup, DC link capacitances were placed between the positive bus and earth, as well as between the negative bus and earth. This strategic inclusion of capacitors creates a low-impedance pathway for potential CM currents to flow through them. Hence, $Z_{src,CM}$ was neglected in the experiments. However, the generality of the results still holds as only the total impedance of $Z_{src,CM}$ and $Z_{line,CM}$ is vital, and not how it is distributed between the two.

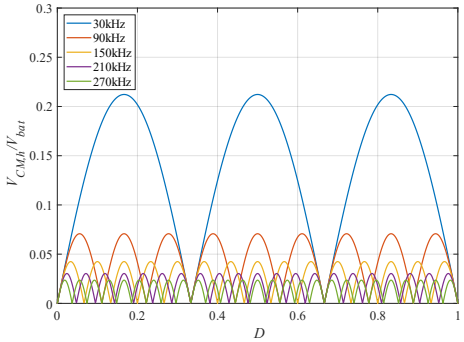


Fig. 8. Variation of v_{CM} harmonics with duty ratio for constant V_{bat}.

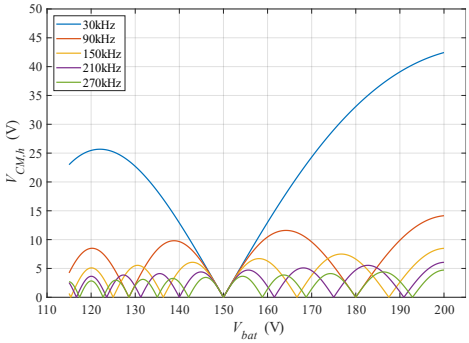


Fig. 9. Variation of v_{CM} harmonics with V_{bat} at V_{DCgrid} =200 V.

$Z_{line,CM}$: This represents the total effective CM impedance resulting from the positive, negative, and earth cables. For the measurement, the cables should be disconnected at both ends from the system, and a short circuit must be established by connecting them together at the DC bus end. Then, the positive and negative cables should be shorted at the charger side. Eventually, the impedance seen from the charger side between the earth cable and the two shorted cables should be measured, which is mainly inductive in nature.

$Z_{y,CM}$: This is the total CM impedance of the charger inverters due to their Y-capacitances. To measure this impedance, the inverter should be isolated by disconnecting the charging cables and the motor from the inverter. Next, the positive terminal of the top inverter DC link should be shorted to the negative terminal of the bottom inverter DC link. Then, the impedance between the shorted terminals and the chassis of the inverter should be measured, which is mainly capacitive in nature.

$Z_{w,CM}$: This is the overall effective CM impedance of the motor winding. For this measurement, one must set up a short circuit between all six motor terminals and then measure the impedance between the shorted terminals and the motor chassis. It is important to emphasize that the inductance of this impedance is not solely represented by L_{ls}/12. Instead, this impedance is primarily capacitive due to the winding capacitance. Its inductive element is considerably smaller compared to the parallel combination of leakage inductances due to the mutual coupling between winding turns. This emphasizes the importance of direct CM impedance measurement rather than relying on calculations based on individual components.

The measured impedances $Z_{line,CM}$, $Z_{y,CM}$, $Z_{w,CM}$ with frequency for the experimental setup are shown in Fig. 10. As expected, it can be observed that $Z_{line,CM}$ and $Z_{y,CM}$ exhibit inductive and capacitive characteristics, respectively. Furthermore, it is noteworthy that $Z_{w,CM}$ is predominantly capacitive as mentioned above, even though it is related to the motor windings.

V. Results

A. Experimental Setup

The experimental setup used to validate the analytical model is shown in Fig. 11(a). A 110kW 10-pole TM4 HSM60-MV255-X1 interior permanent magnet synchronous machine was used as the motor in the experimental system. Two supercapacitor banks of 33.33 F/243 V were used to emulate the battery packs connected to the two inverters. The CM current i_{CM} was measured using a Rogowski coil by passing the positive and negative cables from the DC source through the coil loop (Fig. 11(b)). A resulting experimental CM current waveform is presented in Fig. 12. The controller for the system was implemented on the TI TMSF28379D DSP chip. The controller consisted of a simple zero sequence current regulator with a bandwidth of 14.1 Hz to control the DC charging current. The switching frequency of the inverters was 10 kHz with both vertical and horizontal interleaving.

The procedure used for validating the analytical model is as follows: The supercapacitors were initially pre-charged to a voltage level of 110 V each. Next, the DC charging controller was activated to charge the supercapacitors. The charging current was regulated at 5 A. This current level was selected deliberately to charge the supercapacitors slowly enough to record the CM current waveforms. Considering that the DC charging current level has a negligible effect on the CM currents, its selection does not significantly affect the results. The CM current waveforms were recorded in steps of 5 V starting from 115 V until 200 V, resulting in 18 waveforms. The waveforms were saved as CSV data files for post-processing purposes with a sampling frequency of 8 MHz recorded over a period of 2 ms.

Table II summarizes the parameters of the experimental setup. It is important to note that the values of the parasitic parameters given in Table II are only valid for a single frequency

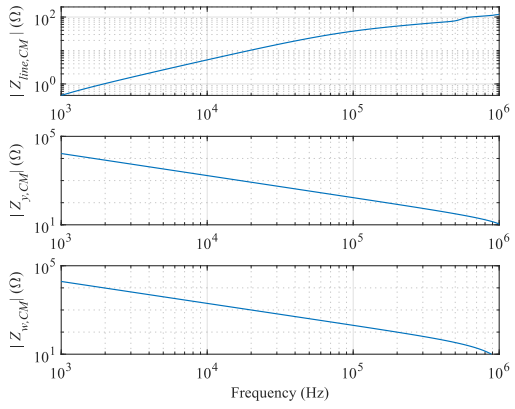
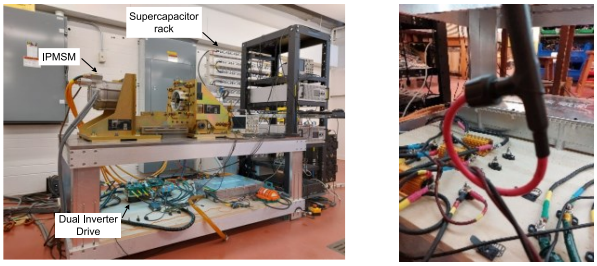


Fig. 10. Measured CM impedances of the experimental system.



(a) (b)

Fig. 11. Experimental setup: (a) Experiment testbench and (b) Rogowski coil.

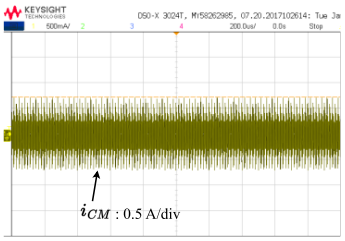


Fig. 12. A measured CM current of the experimental setup.

at which they were measured, which is 270 kHz in this case. These are provided merely to offer a sense of the system and were not used for the analytical calculation of CM currents. Instead, the impedance curves in Fig. 10 were utilized for this purpose. The 0 Ω impedance for $Z_{src,CM}$ indicates the fact that DC bus capacitors were used, shorting any impedance due to the DC supply. Any impedance due to the bus capacitors, albeit very small, was lumped into the $Z_{line,CM}$ measurement (Fig. 10).

TABLE II. Experimental Parameters of the DID-based Integrated DC Charger

Parameter	Symbol	Value
DC source voltage	V_{DC}	200 V
DC charging current	I_{DC}	5 A
Battery pack voltage	V_{bat}	115 – 200 V
Switching frequency	f_{sw}	10 kΩ
Motor winding leakage inductance	L_{ls}	0.47 mH
Motor winding capacitance	C_w	3.49 nF
Inverter y-capacitance	C_y	2.66 nF
Cable CM impedance	$Z_{line,CM}$	60.33∠46.65° Ω
Source CM impedance	$Z_{src,CM}$	~0 Ω

B. Results Comparison

To validate the analytical model, a comparison was conducted between CM currents obtained from analytical calculations, simulations, and the waveforms acquired from experimental data. The analytical calculations were done with equations (7) – (13) using the impedance curves of Fig. 8. However, the calculations were limited to n=17, i.e., all odd triplen harmonics from 30 kHz to 990 kHz. The simulations were performed by implementing the parasitic model of Fig. 6 in PLECS. The parasitic elements used in the simulation were not identical to the lumped parasitic elements of Fig. 6. Instead, combinations of resistors, inductors, and capacitors were used to match the CM impedance profiles of Fig. 10.

The comparisons of the peak and RMS CM currents for the system during DC charging are shown in Fig. 13(a) and Fig.

13(b), respectively. The analytical model demonstrates high accuracy in predicting the experimental values across the entire range of battery pack voltages studied. Furthermore, the best-case and worst-case CM currents are correctly predicted at V_{bat}= 0.75V_{DCgrid} (D=2/3) and V_{bat}=V_{DCgrid}=200 V (D=1/2), respectively.

A perfect alignment is observed in the RMS CM current among the three curves, indicating a high level of precision in the analytical model's CM current predictions. Nevertheless, a small discrepancy emerges in the peak current values, which both the analytical and simulation models underestimate despite their accurate prediction of the peak current trend and the precise RMS current. The following two hypotheses can explain this. First, comparing Fig. 13(a) and Fig. 13(b), we observe that the peak CM current is several times larger than the RMS CM current, i.e., the CM current waveforms have a very high crest factor. This implies that CM waveforms exhibit short-time and sharp peaks whereas during the majority of their duration, the amplitudes remain low. Consequently, the waveform's peak value is primarily determined by only a single data point associated with a sharp peak. This value is highly influenced by the phase relationships among various CM current harmonics. Even a slight phase alteration in a single harmonic component, particularly at higher frequencies, can lead to substantial variations in the peak value. Hence, accurately predicting these peak values is extremely challenging and could account for the observed discrepancy. Another hypothesis that could explain the mismatch is the presence of switching noise, which could introduce abrupt current spikes into the measurements. This phenomenon would explain why the experimental peak current curve in Fig. 13(a) resembles an offsetted version of the analytical curve. Thus, the latter hypothesis provides a stronger explanation for the mismatch. To confirm the analytical model accuracy despite the peak CM current mismatch, a comparative assessment of the individual harmonic components of the CM current waveforms is presented in Fig. 14.

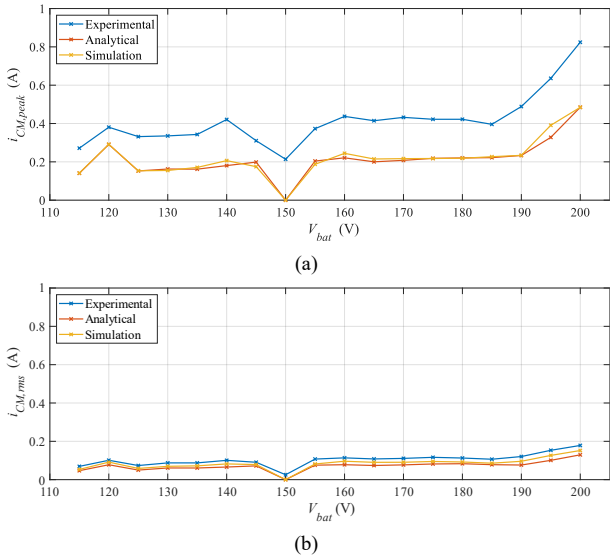


Fig. 13. Comparison of the CM current i_{CM} for DID-based integrated charger: (a) Peak values and (b) RMS values.

The results in Fig. 14 validate the precision of the analytical model, as it is able to capture and match the starkly different trends of the various harmonic components. Hence, the accurate analytical prediction of RMS CM current, as shown in Fig. 13(b), was not coincidental. This further substantiates that the two aforementioned hypotheses are the most viable explanations for the observed offset in the peak CM currents of Fig. 13(a).

To show the qualitative accuracy of the analytical model, a comparative illustration of both the experimental and analytical i_{CM} waveforms is presented in Fig. 15. The time-domain CM current waveforms were obtained for several battery pack voltages, covering different patterns of the current waveform. Evidently, the analytical waveforms accurately capture the salient characteristics of the experimental counterparts, thereby confirming their qualitative precision. The primary distinction between the two waveforms is the prominent current spike superimposed atop the general peak of the experimental

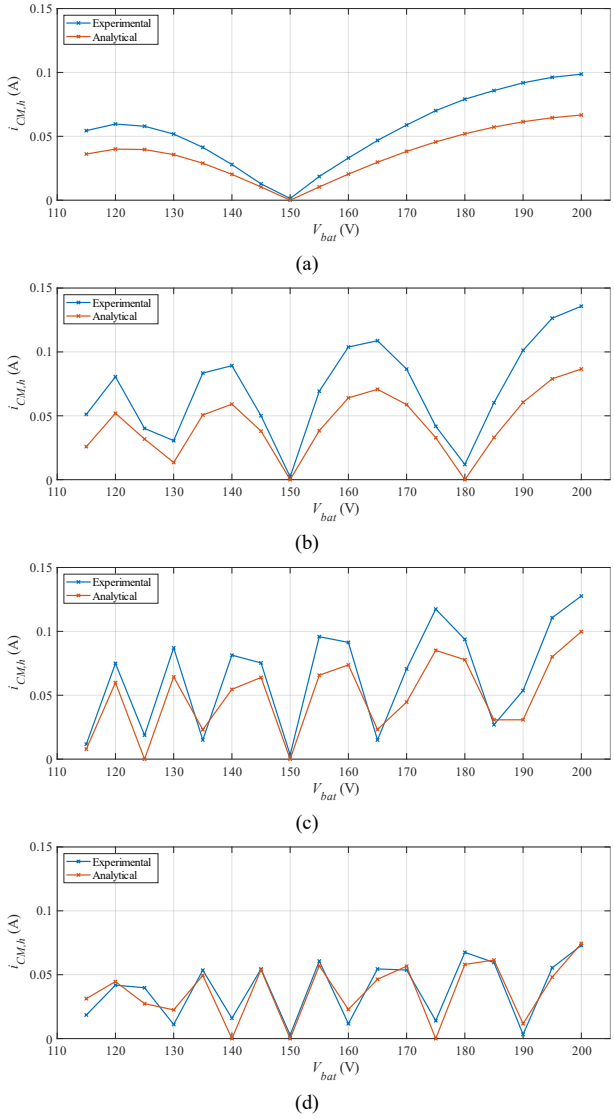


Fig. 14. Comparison of CM current i_{CM} harmonic amplitudes: (a) 30 kHz, (b) 90 kHz, (c) 150 kHz, and (d) 210 kHz.

waveform, which is notably absent in the analytical counterpart. Aside from that, the analytically predicted CM waveform closely mirrors the shape of the experimentally measured one. Since the spikes seem to occur at the same frequency of switching events (60 kHz since there are six switching events per switching cycle), the hypothesis attributing the peak CM current mismatch to switching noise emerges as the most plausible explanation.

Lastly, to verify the standard compliance of the DID-based DC integrated EV charger, the CM current in MIU must be evaluated and compared with the maximum allowed CCID thresholds of the safety standards. According to UL2231, the trip level of 20 MIU must be selected for the CCID employed in a DC FCS with a voltage level over 300 V. Figure 16 represents a comparison of CM currents in MIU (i_{MIU}) that were obtained by filtering the CM currents using the human body model in Fig.

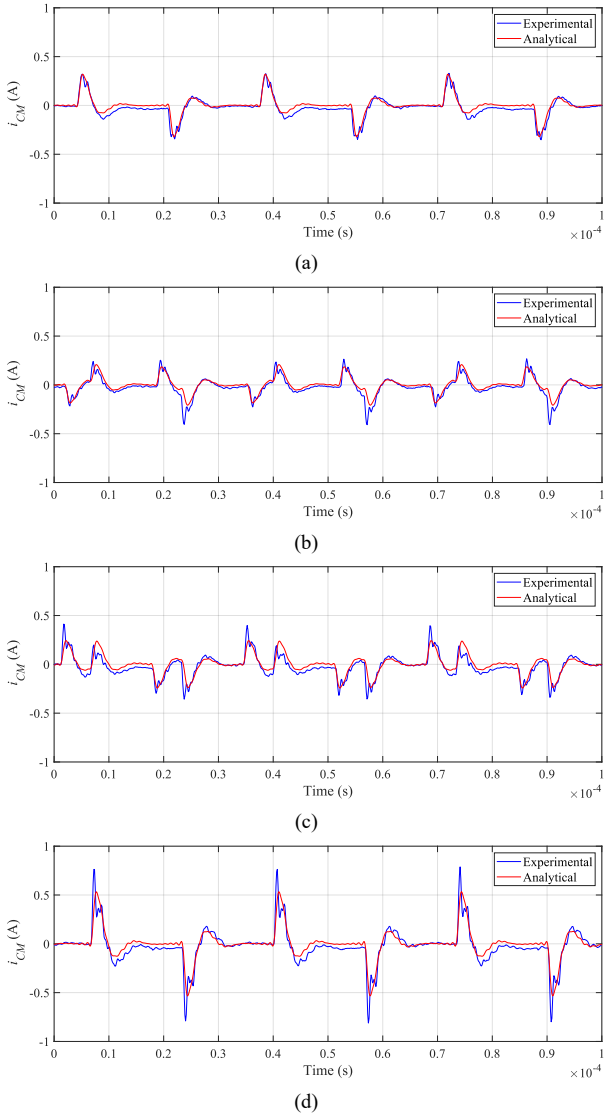


Fig. 15. Comparison of experimental and analytical time-domain waveforms of i_{CM} at (a) V_{bat}= 120 V, (b) V_{bat} = 140 V, (c) V_{bat} = 180 V, and (d) V_{bat} = 200 V.

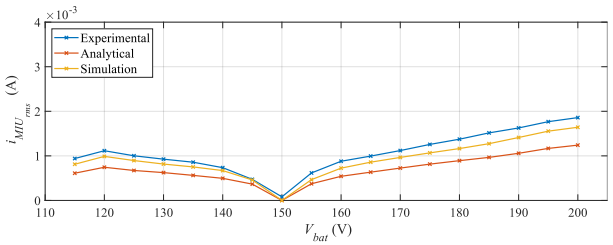


Fig. 16. Comparison of the CM current i_{CM} in RMS MIU for the DID-based integrated charger.

4. The observed maximum CM current in RMS MIU, approximately 1.8 mA, falls comfortably within the permissible threshold by the standard. Nevertheless, it is imperative to note that this result exclusively applies to the system parameters specified in Table II. For a distinct setup, CM currents will inherently differ. The analytical model, however, stands as a valuable tool for predicting the CM current in different systems, provided that the necessary CM impedance data is known.

VI. Conclusion

A comprehensive analytical model for predicting CM currents in a DID-based integrated DC EV charger was presented. Comparison with experimental results shows that the model accurately predicts both quantitative and qualitative aspects of the CM current. Notably, the analysis highlighted the prominent influence of factors such as switching frequency, battery pack voltage, and the ratio of battery pack voltage to the DC grid voltage on the charger CM current. Furthermore, it was deduced that only odd triplen harmonics were present in the CM current. In addition, the CM current observed in the experimental setup remained well below the maximum limits demanded by the safety standards.

This research holds significance as it establishes a clear and fundamental causal link between the charger or operational parameters and the characteristics of CM currents. This allows the designer to predict how the CM currents would be affected due to charger design changes and assess compliance with standard-defined CM current limits. Furthermore, this work emphasizes the importance of explicitly measuring CM impedances and provides guidelines for this.

Moreover, the paper lays the initial framework for analyzing CM currents in a system designed to charge multiple EVs from a common DC bus, a key application enabled by the aforementioned integrated charger. Such knowledge is pivotal for advancing the development and reliability of integrated DC EV chargers in the pursuit of safer and more efficient EV charging systems.

Acknowledgment

This is research work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) under Grant CRDPJ 513206-17.

References

[1] G. Eason M. Yilmaz and P. T. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In

Electric and Hybrid Vehicles," in IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 2151-2169, May 2013.

[2] B. Sarlioglu, C. T. Morris, D. Han and S. Li, "Driving Toward Accessibility: A Review of Technological Improvements for Electric Machines, Power Electronics, and Batteries for Electric and Hybrid Vehicles," in IEEE Industry Applications Magazine, vol. 23, no. 1, pp. 14-25, Jan.-Feb. 2017.

[3] S. Rivera et al., "Charging Infrastructure and Grid Integration for Electromobility," in Proceedings of the IEEE, vol. 111, no. 4, pp. 371-396, April 2023.

[4] Government of Canada. (July 2023). *Net-Zero Emissions by 2050.* [Online]. Available: https://www.canada.ca/en/services/environment/weather/climatechange/climate-plan/net-zero-emissions-2050.html.

[5] M. Weiss, P. Dekker, A. Moro, H. Scholz, and M. K. Patel, "On the electrification of road transportation - A review of the environmental, economic, and social performance of electric two-wheelers," Transp. Res. D, Transp. Environ., vol. 41, pp. 348_366, Dec. 2015.

[6] M. A. H. Rafi and J. Bauman, "A Comprehensive Review of DC Fast-Charging Stations With Energy Storage: Architectures, Power Converters, and Analysis," in IEEE Transactions on Transportation Electrification, vol. 7, no. 2, pp. 345-368, June 2021.

[7] "Electric vehicle conductive charging system - Part 1: General requirements," International Electrotechnical Commission, Standard IEC 61851-1:2017, 2017. [Online]. Available: https://webstore.iec.ch/publication/33644.

[8] "Electric Vehicle and Plug in Hybrid Electric Vehicle Conductive Charge Coupler," Society of Automotive Engineers, Standard SAE J1772:2017, 2017. [Online]. Available: https://www.sae.org/standards/content/j1772_201710.

[9] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii and I. Batarseh, "A Comprehensive Review of Power Converter Topologies and Control Methods for Electric Vehicle Fast Charging Applications," in IEEE Access, vol. 10, pp. 40753-40793, 2022.

[10] J. Wang et al., "Nonisolated Electric Vehicle Chargers: Their Current Status and Future Challenges," in IEEE Electrification Magazine, vol. 9, no. 2, pp. 23-33, June 2021.

[11] M. Y. Metwly, M. S. Abdel-Majeed, A. S. Abdel-Khalik, R. A. Hamdy, M. S. Hamad and S. Ahmed, "A Review of Integrated Onboard EV Battery Chargers: Advanced Topologies, Recent Developments and Optimal Selection of FSCW Slot/Pole Combination," in IEEE Access, vol. 8, pp. 85216-85242, 2020.

[12] I. Subotic, N. Bodo and E. Levi, "An EV Drivetrain With Integrated Fast Charging Capability," in IEEE Transactions on Power Electronics, vol. 31, no. 2, pp. 1461-1471, Feb. 2016.

[13] C. Shi, Y. Tang and A. Khaligh, "A Three-Phase Integrated Onboard Charger for Plug-In Electric Vehicles," in IEEE Transactions on Power Electronics, vol. 33, no. 6, pp. 4716-4725, June 2018.

[14] R. Shi, S. Semsar and P. W. Lehn, "Constant Current Fast Charging of Electric Vehicles via a DC Grid Using a Dual-Inverter Drive," in IEEE Transactions on Industrial Electronics, vol. 64, no. 9, pp. 6940-6949, Sept. 2017.

[15] S. Semsar, T. Soong and P. W. Lehn, "Onboard Single-Phase Integrated Electric Vehicle Charger With V2G Functionality," in IEEE Transactions on Power Electronics, vol. 35, no. 11, pp. 12072-12084, Nov. 2020.

[16] C. Perera, M. Pathmanathan, C. Viana and P. W. Lehn, "Active Power Decoupling Strategy for Single Phase AC Charging Using a Dual Inverter Drive," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1680-1687.

[17] "Personnel Protection Systems for Electric Vehicle (EV) Supply Circuits; Part 1: General Requirements," Underwriters Laboratories Inc., Standard UL 2231-1, 2021. [Online]. Available: https://www.shopulstandards.com/ProductDetail.aspx?UniqueKey=24886.

[18] "Personnel Protection Systems for Electric Vehicle (EV) Supply Circuits: Particular Requirements for Protection Devices for Use in Charging Systems," Underwriters Laboratories Inc., Standard UL 2231-2, 2021. [Online]. Available: https://www.shopulstandards.com/ProductDetail.aspx?UniqueKey=24887.

[19] C. Viana, S. Semsar, M. Pathmanathan and P. W. Lehn, "Integrated Transformerless EV Charger With Symmetrical Modulation," in IEEE Transactions on Industrial Electronics, vol. 69, no. 12, pp. 12506-12516, Dec. 2022.

[20] A. D. Brovont and S. D. Pekarek, "Derivation and Application of Equivalent Circuits to Model Common-Mode Current in Microgrids," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 297-308, March 2017.