A Modular Multilevel DC–DC Converter With Flying Capacitor Converter Like Properties

Philippe A. Gray, *Graduate Student Member, IEEE*, Peter W. Lehn, *Senior Member, IEEE*, and Netan Yakop, *Graduate Student Member, IEEE*

***Abstract*—This article proposes a novel modular multilevel dc-dc converter with high power-density potential based on a cascaded string of voltage source submodules (VSMs) merged with a current source submodule (CSM) that is configured to rapidly invert the polarity of the current in the VSM string. The proposed hybrid converter combines the modularity advantages of the modular multilevel converter (MMC) and the high effective frequency advantages of the flying capacitor converter. Unlike other hybrid nonisolated MMC structures the proposed converter features a novel CSM stage enabling a near 50% reduction in string current, and the input source and output load to be commonly grounded. In addition, the proposed operational approach enables self-balancing of the VSMs and a simple overall control structure. This article introduces the main operating principles of this novel topology termed the current shaping modular multilevel forward converter along with a proposed control design. A peak efficiency of 97.1% is measured from a laboratory-scale prototype at 950-137V and 1.45 kW.**

***Index Terms*—Modular multilevel converter (MMC), dc–dc converter, high-frequency, self-balancing, high step ratio, MVDC, current shaping.**

I. Introduction

MULTILEVEL dc–dc converters enable the delivery of power from a medium voltage dc (MVDC) grid to a low voltage dc (LVDC) load. A MVDC grid is defined by CIGRE Working Group SC6.31 as a grid with a voltage between 1.5 kV and 100 kV [1]. Examples of LVDC loads include 380 Vdc households, dc street lighting systems, electric vehicles (EVs), and auxiliary loads for electric trains.

Modular multilevel converter (MMC) structures are commonly proposed for MVDC grid applications. MMC structures are advantageous as they can be adapted for a wide range of input voltages simply by increasing the total number of cascaded voltage source submodules (VSMs). State-of-the-art MMC topologies for dc–dc applications (dc–dc MMCs) include the front-to-front MMC (F2F-MMC) [2], the HVDC autotransformer (HVDC-AT) [3], the modular multilevel dc converter (M2DC) [4]–[7] and the hybrid cascaded dc–dc converter (HCDC) [8].

A common drawback of the state-of-the-art dc–dc MMCs is that they all require arm inductors that are electrically in series with the VSMs to limit currents from circulating between legs of the converter and to limit the propagation of fault currents. Due to the high ac voltage drop across the arm inductors at elevated frequencies, as well as switching loss considerations, the ac component of the arm currents, termed the circulating ac current, is limited to relatively low frequencies. In high voltage dc (HVDC) applications, the circulating ac current is typically limited to a few hundred Hz, dominated by the high number of switching operations [9]. This circulating ac current is required to restore energy balance in the VSM capacitors. Consequently, to manage the ripple voltage of the VSM capacitors, relatively high VSM capacitances are required. The M2DC, HVDC-AT, and HCDC structures have additional drawbacks including high blocking voltage requirements, a high number of switching operations since all VSMs are switched at least once in each ac period, multiple parallel strings, and no galvanic isolation capability. For a modulation index of $m_a = 1$, the total blocking voltage per VSM string for the HVDC-AT and M2DC is $2v_H$ [10], where v_H represents a dc grid voltage. Furthermore, the transformer of the HVDC-AT is subjected to high dc voltage stresses and while the M2DC does not require a transformer it has high output filtering requirements. As noted in [10], the M2DC and the HVDC-AT converters are particularly well suited for low to moderate conversion ratio applications.

To improve the power density of MMC structures, both novel control approaches [11]–[13] and resonant dc-dc topologies such as [14]–[17] have been proposed to increase the frequency of the circulating ac current. In the quasi-two-level control approach of [11], the MMC operates similarly to a two-level voltage source converter, switching in VSMs to support the transition between the two voltage levels. Due to the relatively short transition periods, the VSM capacitor voltage ripple can be managed with reduced VSM capacitances than that employed in traditional MMC converters, as noted in [11]. However, the intermediate transformer is subjected to increased stresses due to the faster *dv/dt* rates and additional harmonics [18]. In the resonant approaches such as [14]–[17], circulating ac currents at elevated frequencies can be achieved, however, resonant converters

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The authors are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada. (e-mail: p.gray@mail.utoronto.ca; lehn@ece.utoronto.ca; netan.yakop@mail.utoronto.ca).

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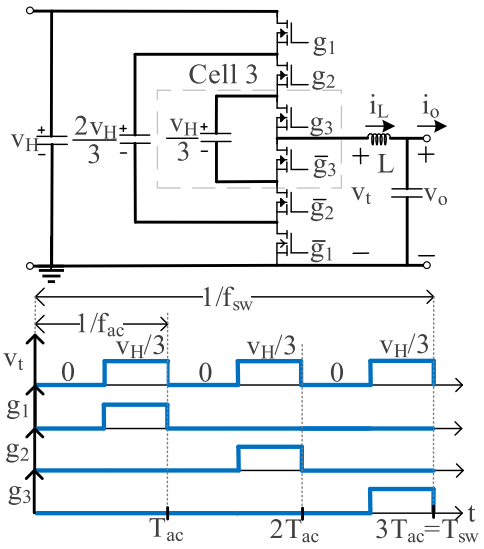

Fig. 1. A Three-Cell, Four-Level Flying Capacitor Converter. Topology and representative waveforms.

feature drawbacks such as higher peak stresses [19], higher component stress, and increased circuit and control complexity.

In comparison to the previously mentioned approaches, the flying capacitor converter (FCC), proposed in [20], is a non-resonant multilevel converter topology that, while not modular, is inherently able to circulate higher frequency ac currents at low blocking voltages with relatively low switching losses. For illustrative purposes, a three-cell, four-level FCC is illustrated in Fig. 1 along with representative waveforms of the terminal voltage v_t and the gating pulses to the upper three switches g_1, g_2 and g_3. The lower switches receive complementary gating pulses. An FCC cell consists of two switches and a capacitor. One FCC cell is highlighted in Fig. 1. Inductor L carries a dc current in the direction indicated by its respective arrow.

The FCC achieves high effective frequencies due to its switching frequency multiplicative property and its ability to near-instantly change the direction of the current delivered to the flying capacitors.

i) As can be observed in Fig. 1, while the FCC switches are switched at a frequency of $f_{\rm sw}$, the frequency of the terminal voltage v_t is at $f_{\rm ac} = 3f_{\rm sw}$. Therefore, the frequency of the ripple current for inductor L is $3f_{\rm sw}$. In general, for a N cell FCC, the ripple frequency is $Nf_{\rm sw}$. The advantage of this switching frequency multiplicative effect was demonstrated in [21] for an 800Vdc application enabling a ripple frequency of 1.44MHz to be achieved.

ii) In the FCC, the conduction path for the inductor current i_L is changed via switch action. Since there is no inductor within any FCC cell, the inductor current i_L can be commutated between the upper and lower switch of an FCC cell nearly instantly.

Recently, a new class of MMC structures has been proposed termed the current shaping MMC (CS-MMC) [22]–[24]. Like the FCC, the CS-MMC features a switching frequency multiplicative property and the ability to near-instantly change the direction of the current delivered to the VSM capacitors through its use of a current source module (CSM) stage. While [22]–[24] demonstrate the energy transfer mechanism underlying the CS-MMC, the original topology features two major drawbacks when compared to the FCC. First, a large voltage appears at the neutral of the output due to the switching action of the CSM, whereas in the FCC the input and output are commonly grounded. Second, the control is relatively complex requiring active regulation of the VSM capacitor voltages. In the FCC, natural self-balancing of the cell capacitors can be achieved as demonstrated in [25]. Self-balancing greatly simplifies the hardware requirements when compared to the active capacitor balancing approaches developed for MMC topologies, some of which are detailed in [26].

TABLE I
COMPARING THE FCC AND CS-M2FC

	FCC	CS-M2FC
Modular	No	Yes
String RMS Current	I_o	$<0.56I_o$[a]
Galvanic Isolation Capability	No	Yes
Number of Cells	N	N
Blocking Voltage of Cell Switches	$\frac{1}{N}V_H$	$\frac{1}{N-1}V_H$
Blocking Voltages of Cell Capacitors	V_H, $\frac{(N-1)}{N}V_H,\ldots,\frac{1}{N}V_H$	$\frac{1}{N-1}V_H$
Ripple Frequency	$Nf_{\rm sw}$	$N/2f_{\rm sw}$
Input Filtering Requirements	Smaller	Greater

[a]This represents a worst-case rms current conducted by the VSM switches in the CS-M2FC.

In this article, a new topology and operational approach are proposed for the CS-MMC family. This topology is particularly well suited for tapped power applications. The envisioned application is to transfer 10–100s of kW of power from a medium voltage dc distribution network to a low voltage dc load. The topology is termed the current shaping modular multilevel forward converter (CS-M2FC). Compared to the original work in [22], the proposed converter has the following advantages: a near 50% reduction in string current; common input and output grounding; galvanic isolation potential; and self-balancing of the VSM capacitor voltages.

A high-level comparison of the FCC and the CS-M2FC topologies is given in Table I. This article is structured by first presenting the CS-M2FC topology. Then, a high-level overview of the energy transfer mechanism underlying the topology is provided. This is followed by a detailed overview of the operating concepts. Next, the dynamic circuit analysis is presented. This is then followed by an overview of the controller implementation which is followed by a discussion on converter design considerations. Experimental results are then presented from a 1000–145 Vdc, 3.7 kW laboratory-scale prototype featuring an effective frequency of 50 kHz.

II. Converter Architecture and Features

The proposed CS-M2FC topology is provided in Fig. 2. The converter interfaces a higher voltage dc input source v_H to a

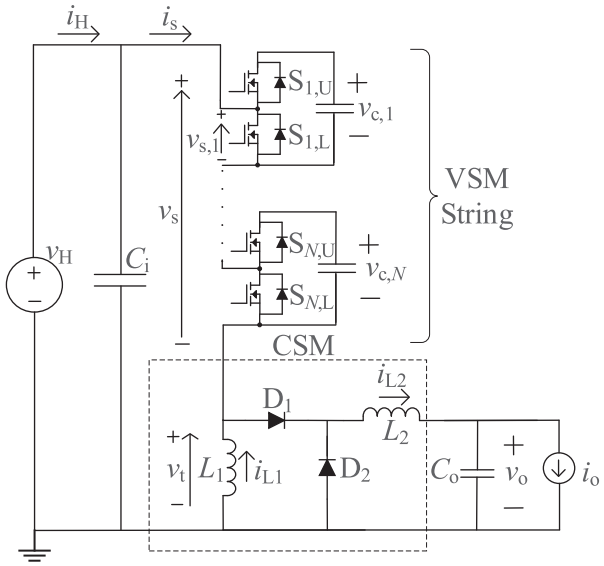

Fig. 2. Proposed CS-M2FC topology.

lower voltage dc output, v_o. The structure consists of a VSM string and a CSM. The VSM string consists of N VSMs of half-bridge type. Note, in this article, while describing the CS-M2FC, the terms VSM and cell are used interchangeably. The dc load is considered in this article to be a current source, which is denoted i_o. Across the input voltage source and the dc load are capacitors C_i and C_o which are required for high-frequency filtering purposes. The net output voltage of the VSM string is denoted v_s. The advantageous features enabled by the novel CSM stage are detailed next.

A. Common Ground

The CSM features two diodes, two inductors, and a common neutral between v_H and v_o, allowing the input and output to share a common ground. The maximum voltage applied across the input terminals of the CSM is equal to one cell capacitor voltage, denoted v_c. Therefore, only low voltages are applied across the CSM stage. Conversely, in [22]–[24] the input and output cannot share a common ground due to the diode bridge stage.

Both CSM inductors, L_1 and L_2 carry a dc current in the direction indicated by their respective arrows in Fig. 2.

B. Reduced VSM String Current

In typical nonisolated converters including the original CS-MMC topology of [22], the VSMs must conduct the full output current, i_o. In high conversion ratio applications, the VSM string is comprised of many VSMs and therefore this can lead to elevated string conduction loss. In this topology, due to the arrangement of the diodes and the use of two inductors in the CSM, the VSMs conduct only a fraction of the output current. The rms current conducted by the VSMs will be less than 0.56 i_o (refer to Section VII.C) yielding a corresponding reduction in string conduction losses.

C. Self-Balancing of VSM Capacitor Voltages

Since inductor volt-second balance is a necessary condition for steady-state operation, inductor L_1 imposes a zero-dc voltage across the input terminals of the CSM. This structural feature combined with the modulation scheme proposed in Section IV, ensures that the VSM capacitor voltages are balanced and passively regulated. Consequently, no cell capacitor voltages need to be measured in the approach proposed in this article.

D. Potential for Galvanic Isolation

As a zero-dc voltage is imposed across the input terminals of the CSM, it is possible to replace the inductor L_1 by a transformer, where L_1 would then correspond to the magnetizing inductance of the transformer. In comparison, the operational approaches proposed in [22]–[24] inherently impose a nonzero dc voltage across the input terminals of the CSM, and therefore galvanic isolation is not possible. However, isolation is beyond the scope of this article and therefore is not discussed further.

III. Energy Transfer Mechanism

The three states of the converter are graphically presented in Fig. 3(a)–(c) and are referred to as states 1, 2, and 3, respectively. The total number of inserted cells in states 1, 2, and 3 are $N-2$, N, $N-1$, respectively. The dashed lines in Fig. 3 represent common current paths. While the converter has three states, it is only in states 1 and 2 that power is delivered to the CSM inductors. The state of the converter is determined by the voltage applied across the input terminals of the CSM. If it is assumed that all VSM capacitors are reasonably well balanced, i.e., $v_{c,i} \approx v_{c,j} = v_c$, for $\forall i, j \in [1, N]$, the applied voltage v_t can be defined by the following expression:

$$v_t\ (t) = v_H\ - n\,(t)\, v_c\,(t) \tag{1}$$

where $n(t) \in [0, N]$ represents the total number of cells inserted at time t; and v_c represents a cell capacitor voltage at time t. Taking cell 1 in Fig. 2 as an example, if the upper switch, $S_{1,U} = 1$ and the lower switch, $S_{1,L} = 0$ then cell 1 is inserted and the output voltage of cell 1 is $v_{s,1} = v_{c,1}$. Conversely, if $S_{1,L} = 1$ and $S_{1,U} = 0$, then cell 1 is bypassed and the output voltage of cell 1 is $v_{s,1} = 0$.

If the total number of inserted VSMs is sufficiently low, a positive voltage will be imposed across the input terminals of the CSM, i.e., $v_t > 0$. In this case, the converter operates in state 1, shown in Fig. 3(a). In state 1, power is delivered to the CSM inductor L_2.

Alternatively, if the total number of inserted VSMs is sufficiently high, a negative voltage will be applied across the input terminals of the CSM, i.e., $v_t < 0$, and the converter operates in state 2, shown in Fig. 3(b). In state 2, power is delivered to CSM inductor L_1.

In state 1, the string current is positive, and in state 2, the string current is negative. Therefore, in state 1 the cell capacitors of the inserted VSMs are charged and in state 2 the cell capacitors of the inserted VSMs are discharged. By alternating between states

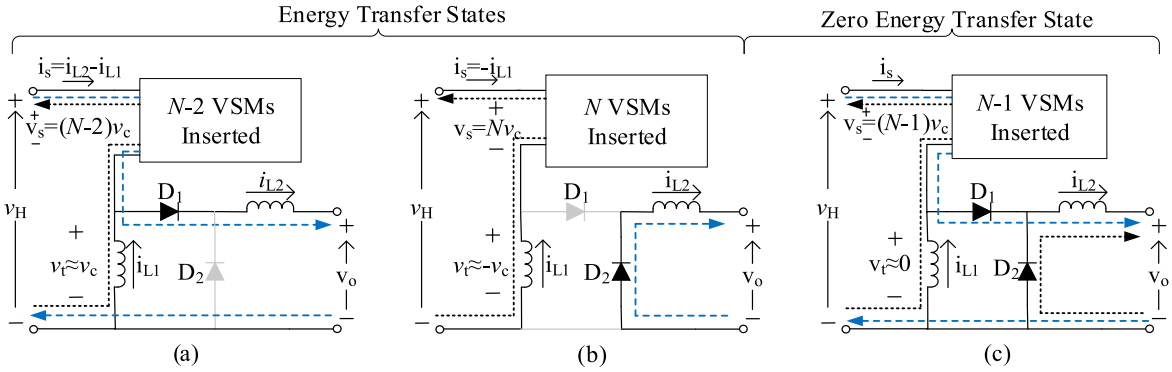

Fig. 3. Operating states of the converter.

1 and 2, it is possible to deliver near-continuous power to the CSM, all while ensuring voltage balance of the cell capacitors.

There is also a third converter state in which only negligible power is delivered to the CSM. This state is represented in Fig. 3(c) and is referred to as state 3. In this state, the voltage appearing across the input terminals of the CSM is near zero, i.e., $v_t \approx 0$. Since only negligible power is delivered to the CSM in this state, it is possible to modulate the power being delivered to the CSM by adjusting the relative duration of state 3 with respect to the relative durations of states 1 and 2. The relative durations of states 1 and 2 are by construction equivalent which ensures that on average there are $N-1$ VSMs inserted. Since the dc component of the applied voltage is zero, i.e., $V_t = 0$, the following expression for the average cell capacitor voltage V_c can be readily obtained from (1),

$$V_c = \frac{V_H}{N-1} \tag{2}$$

where V_H is the steady-state value of v_H.

The relative durations of states 1–3 are defined as d, d, and $1-2d$, respectively. The variable $d \in [0, 0.5]$ represents a duty ratio term. The duty ratio term is the only control variable for this converter. By varying the duty ratio d, the converter can be adapted for a wide range of conversion ratios. The conversion ratio for the converter is defined as follows:[1]

$$\frac{V_o}{V_H} = \frac{D}{N-1}\,. \tag{3}$$

Since the duty ratio, D can be varied within the range $[0, 0.5]$, the converter can regulate any output voltage, $0 \le V_o \le 0.5V_H/(N-1)$.

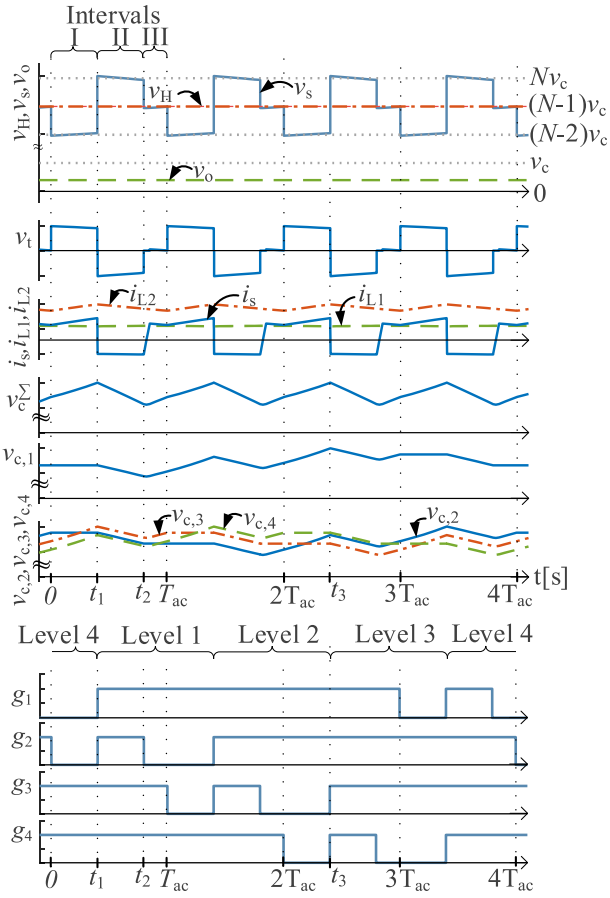

Fig. 4. Representative steady-state operating waveforms based on four VSMs. A total of four fundamental ac periods is shown.

IV. Operating Concepts

Representative operating waveforms for a converter with $N = 4$ VSMs are provided in Fig. 4. Note, as per (2) the blocking voltage of each VSM switch is $V_H/3$ when $N = 4$. The blocking voltage of each FCC switch in the three-cell, four-level FCC of Fig. 1 is also $V_H/3$ (per Table I). The operating waveforms of Fig. 4 have a periodicity of $NT_{\rm ac}$; where $T_{\rm ac}$ represents the fundamental period of the string current i_s. The fundamental ac frequency is denoted $f_{\rm ac} = 1/T_{\rm ac}$. The net output voltage of the VSM string v_s is a three-level voltage waveform. This waveform is provided in the top plot of Fig. 4.

The gating signals are labeled as g_1, g_2, g_3, and g_4 in Fig. 4. These signals are delivered to the upper switches of VSMs 1–4, respectively, (the lower VSM switches receive complimentary gating signals). The gating signals delivered to each VSM are equivalent, but phase displaced by $T_{\rm ac}$. To generate these signals,

[1]This expression can be derived by applying volt-second balance to inductor L_2 using the expressions derived in (7a), (12a), and (15a).

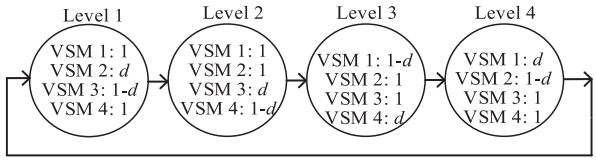

Fig. 5. Four-level state machine for $N = 4$ VSMs. The duty ratio for the upper switch of each VSM is specified for each sate machine level. The state machine level is updated every $T_{\rm ac}$.

a state machine is employed. This state machine is illustrated in Fig. 5. The state machine bears similarity to that first introduced for self-balanced flying capacitors in [25] and later for MMCs [27]. A state machine ensures that all cell capacitor voltages are balanced with respect to each other.

As can be observed from gating signals g_1, g_2, g_3, and g_4 over $NT_{\rm ac}$ there are two switching cycles per VSM. If the switching frequency of a VSM is denoted $f_{\rm sw}$ then the fundamental ac frequency of the converter is related to $f_{\rm sw}$ by the following expression:

$$f_{\rm ac} = \frac{N}{2} f_{\rm sw}. \tag{4}$$

Therefore, an advantageous frequency multiplicative effect occurs whereby the fundamental ac frequency of the converter is a $N/2$ multiple of the switching frequency of a VSM. This is a similar phenomenon to that experienced by the FCC enabling it to achieve high ripple frequencies without incurring high switching loss.

Each fundamental ac period is characterized by three distinct intervals. Intervals I–III are labeled at the top of Fig. 4 and are detailed next.

Interval I [see Fig. 3(a), from $t = 0$ to $t_1 = dT_{\rm ac}$]: In interval I, the converter operates in state 1, which is shown in Fig. 3(a). There are a total of $N - 2$ VSMs are inserted in this interval. The net output of the VSM string is $v_s = (N - 2)\, v_c$. The voltage imposed across the input terminals of the CSM is positive and equal to the following:

$$v_t \approx v_c. \tag{5}$$

Due to the positive voltage, CSM diode D_1 is forward biased and diode D_2 is reverse biased. In this state, the string current is positive and defined as follows:

$$i_s = i_{L2} - i_{L1}. \tag{6}$$

For this interval, differential equations for i_{L1} , i_{L2} and for the total sum of all cell capacitor voltages, v_c^{Σ} can be obtained from inspection of Fig. 3(a). From $t = 0$ to $dT_{\rm ac}$,

$$L_2 \frac{di_{L2}}{dt} = v_H - \frac{N-2}{N} v_c^{\Sigma} - v_o \tag{7a}$$

$$L_1 \frac{di_{L1}}{dt} = \frac{N-2}{N} v_c^{\Sigma} - v_H \tag{7b}$$

$$C \frac{dv_c^{\Sigma}}{dt} = (N-2)\,(i_{L2} - i_{L1}) \tag{7c}$$

where v_c^{Σ} is defined as follows:

$$v_c^{\Sigma} = \sum_{i=1}^{N} v_{c,i}\ . \tag{8}$$

Assuming that the cell capacitor voltages are well balanced, the cell capacitor voltage, v_c, is related to v_c^{Σ} as follows:

$$v_c = \frac{v_c^{\Sigma}}{N}. \tag{9}$$

Interval II [see Fig. 3(b), from $t_1 = dT_{\rm ac}$ to $t_2 = 2dT_{\rm ac}$]: In interval II, the converter operates in state 2, shown in Fig. 3(b). There are a total of N cells inserted in this interval. The net output of the VSM string is $v_s = Nv_c$ and the voltage appearing across the input terminals of the CSM is negative and given by,

$$v_t \approx -v_c. \tag{10}$$

Due to this negative voltage, the diode D_2 is forward biased and diode D_1 is reverse biased. In this state, the string current is negative and defined as follows:

$$i_s = -i_{L1}. \tag{11}$$

Differential equations for i_{L1}, i_{L2} and v_c^{Σ} for this interval can be obtained from Fig. 3(b). From $t = dT_{\rm ac}$ to 2 $dT_{\rm ac}$,

$$L_2 \frac{di_{L2}}{dt} = -v_o \tag{12a}$$

$$L_1 \frac{di_{L1}}{dt} = v_c^{\Sigma} - v_H \tag{12b}$$

$$C \frac{dv_c^{\Sigma}}{dt} = -Ni_{L1}. \tag{12c}$$

Interval III [see Fig. 3(c), from $t_2 = 2dT_{\rm ac}$ to $T_{\rm ac}$]: In interval III, the converter operates in state 3 of Fig. 3(c). There are a total of $N - 1$ inserted VSMs and the net output of the VSM string is $v_s = (N - 1)\, v_c$. The voltage appearing across the input terminals of the CSM is,

$$v_t \approx 0. \tag{13}$$

While the imposed voltage is near to zero, due to the cell capacitor voltage ripple, v_t is a small positive value throughout this interval. In this interval, the string current is clamped by the CSM to the following value:

$$i_s = i_{L2} - i_{L1}. \tag{14}$$

Differential equations for i_{L1} and i_{L2} and v_c^{Σ} can be obtained by inspection of Fig. 3(c). From $t = 2dT_{\rm ac}$ to $T_{\rm ac}$,

$$L_2 \frac{di_{L2}}{dt} = -v_o \tag{15a}$$

$$L_1 \frac{di_{L1}}{dt} = \frac{N-1}{N} v_c^{\Sigma} - v_H \tag{15b}$$

$$C \frac{dv_c^{\Sigma}}{dt} = (N-1)\,(i_{L2} - i_{L1})\,. \tag{15c}$$

At the end of each fundamental ac period, denoted $T_{\rm ac}$, inductors L_1 and L_2 achieve inductor volt-second balance and

the total sum of cell capacitor voltages, v_c^{Σ}, achieves capacitor charge balance. This can be observed in the plots of i_{L1}, i_{L2}, and v_c^{Σ}, respectively. Every N fundamental ac periods, i.e., $NT_{\rm ac}$, the individual cell capacitor voltages, $v_{c,1}, v_{c,2}, v_{c,3}$, and $v_{c,4}$ achieve charge balance as can be observed in Fig. 4.

It can also be observed from the string current waveform, like FCC, the proposed topology can near-instantly reverse the polarity of the current into the VSM capacitors simply through converter switch action. The polarity of the string current is reversed by changing the total number of inserted VSMs.

V. Dynamic Circuit Analysis

In this section, expressions for v_o and i_{L2} are derived in terms of transfer functions. These expressions are required in developing the controller proposed for this converter.

The differential equation describing the output capacitor voltage can be obtained by inspection of Fig. 2. The result is the following:

$$C_o \frac{dv_o}{dt} = i_{L2} - i_o. \tag{16}$$

Equation (16) can be expressed in transfer function form as follows:

$$v_o\ (s) = \frac{1}{sC_o}\ (i_{L2}\,(s) - i_o\,(s))\,. \tag{17}$$

To derive a dynamic expression for inductor L_2, a state-space averaging approach is employed. The relevant differential equations are (7a), (12a) and (15a). By applying state-space averaging, the following time-averaged expression results:

$$L_2 \frac{d\langle i_{L2}\rangle_{T_{\rm ac}}}{dt} = \langle d\rangle_{T_{\rm ac}} \left(\langle v_H\rangle_{T_{\rm ac}} - \frac{N-2}{N}\langle v_c^{\Sigma}\rangle_{T_{\rm ac}}\right) - \langle v_o\rangle_{T_{\rm ac}} \tag{18}$$

where $\langle\cdot\rangle_{T_{\rm ac}}$ represents the time-average over a fundamental ac period, T_{ac}. As an example, $\langle i_{L2}\rangle_{T_{\rm ac}} = I_{L2} + \hat{i}_{L2}$; where $\hat{i}_{L2}$ represents the small-signal quantity of i_{L2} and I_{L2} represents the large-signal quantity of i_{L2}.

If (18) is linearized, and (2) and (9) are substituted in, (18) can be expressed in transfer function form as follows:

$$\hat{i}_{L2}\,(s) = \frac{1}{sL_2}\left(V_c\hat{d}\,(s) + D\hat{v}_H\,(s) - \frac{D\,(N-2)}{N}\hat{v}_c^{\Sigma}\,(s) - \hat{v}_o\,(s)\right) \tag{19}$$

where $\hat{(\cdot)}$ designates a small signal quantity.

VI. Control Model

Based on the dynamic equations of (17) and (19), the control block diagram of Fig. 6 is derived. This diagram presents the proposed controller along with a plant model. Since no cell capacitor voltages are measured, the term v_c^{Σ} in Fig. 6 is considered as a disturbance to be rejected by the controller.

The controller features both a faster inner current control and slower outer voltage control. The measured inputs are the output voltage v_o, the inductor current i_{L2} and the load current i_o. The blocks denoted "PI" correspond to proportional integral controllers. The controller regulates the output voltage v_o by adjusting the duty ratio d. The gating signals for the N VSMs are generated based on the duty ratio d and the current level of the state machine (an illustration of which was provided in Fig. 5). The level of the state machine is updated once per fundamental ac period.

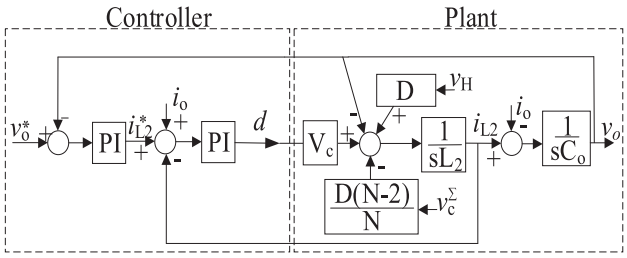

Fig. 6. Block diagram of proposed controller and the plant.

VII. Converter Design

This section provides additional design equations to support the circuit designer in rating the CSM and the VSM components.

A. CSM Inductor L_2 Rating

The steady-state current value of the inductor L_2 is as follows:

$$I_{L2} = I_o\,. \tag{20}$$

Equation (20) is obtained by applying charge balance to (16).

The inductor L_2 inductance can be selected based on the following equation:

$$L_2 = \frac{V_o}{\Delta i_{L2} f_{ac}}\left(1 - \frac{V_o}{V_H}\,(N-1)\right) \tag{21}$$

Where Δi_{L2} represents the peak-to-peak ripple current of the inductor L_2. This expression is obtained by applying (2), (3), (9), (12a) and (15a) to the fundamental inductor relation (i.e., $v_{L2} = L_2\, di_{L2}/dt$). For the experimental prototype of this article, the L_2 inductance is selected such that the peak-to-peak ripple current is 40%. This design choice was made considering VSM switch ratings as well as VSM switching and conduction losses.

B. CSM Inductor L_1 Rating

The steady-state current value of the inductor L_1 can be derived by applying capacitor charge balance to the input capacitor C_i. The differential equation is the following:

$$C_i \frac{dv_{ci}}{dt} = i_H\ (t) - i_s\,(t)\,. \tag{22}$$

To apply capacitor charge balance to (22), the string current, i_s, must be defined over one fundamental ac period.

In Fig. 4, the string current is well defined over a fundamental ac period. However, in general, the string current is not well defined in interval III due to the additional current loop formed by the two conducting diodes in state 3 as shown in Fig. 3(c). The

string current value in interval III depends on the *RLC* circuit formed by the inserted VSM capacitors, stray loop inductance, and the equivalent resistance of the VSM string as well as the duty ratio D. The string current is however restricted to the range $i_s \in [-i_{L1}, i_{L2} - i_{L1}]$ due to the clamping action of the CSM. In a well-designed converter, the duty ratio will be near to 0.5 to minimize the energy stored within the converter. For a duty ratio near 0.5, the string current can be approximated as $I_s = I_{L2} - I_{L1}$ in interval III as illustrated Fig. 4. This approximation also represents the worst-case in terms of component ratings and therefore is considered in this article for rating the converter components.

If capacitor charge balance is applied to (22) over a fundamental ac period and considering a string current in interval III equal to $I_s = I_{L2} - I_{L1}$, the following is obtained:

$$0 = I_H - \overbrace{(1-D)(I_{L2}-I_{L1})}^{\text{Interval I+Interval III}} + \overbrace{DI_{L1}}^{\text{Interval II}}. \quad (23)$$

If (3), (20) and $I_H = I_o\, V_o/V_H$ (obtained from power balance) are substituted into (23), the following expression for I_{L1} is obtained,

$$I_{L1} = I_o \left(1 - \frac{NV_o}{V_H}\right). \quad (24)$$

Equation (24) provides the steady-state inductor L_1 current.

The inductance of the inductor L_1 can be selected based on the following expression:

$$L_1 = \frac{V_o}{\Delta i_{L1} f_{\text{ac}}} \quad (25)$$

Where, Δi_{L1} represents the peak-to-peak ripple current of the inductor L_1. This expression is obtained by substituting (2), (3), (9), and (7a) into the fundamental inductor relation (i.e., $v_{L1} = L_1\, di_{L1}/dt$).

C. VSM Rating

The VSM capacitor capacitance can be selected by the following equation:

$$C = \frac{I_o}{\Delta v_c f_{\text{ac}}} \left(N \left(\frac{V_o}{V_H}\right)^2 (1-N) - \frac{V_o}{V_H}(3-2N) \right) \quad (26)$$

Where Δv_c represents the peak-to-peak ripple voltage of a VSM capacitor voltage. This expression for the $N = 4$ case can be obtained from Fig. 4 by applying the fundamental capacitor relation (i.e., $i_{c,1} = C dv_{c,1}/dt$) to the capacitor of VSM 1 over the interval $t_2 = 2dT_{\text{ac}}$ to $t_3 = (2+d)T_{\text{ac}}$.

An expression for the rms string current, $I_{s,\text{rms}}$, can be derived as follows:

$$I_{s,\text{rms}} = \sqrt{\overbrace{(1-D)(I_{L2}-I_{L1})^2}^{\text{Interval I+Interval III}} + \overbrace{D(I_{L1})^2}^{\text{Interval II}}}. \quad (27)$$

Where (27) considers a string current in interval III equal to $I_s = I_{L2} - I_{L1}$. If (3), (20), and (24) are substituted into (27), the following simplified expression for the rms string current is obtained,

$$I_{s,\text{rms}} = I_o \sqrt{\frac{V_o}{V_H}} \sqrt{(N-2)\left(1 - \frac{NV_o}{V_H}\right) + 1}. \quad (28)$$

Since $0 \le V_o \le 0.5V_H/(N-1)$ by (3), it is possible to determine from (28), that $I_{s,\text{rms}} < 0.56 I_o$ for all possible values of N, V_o and V_H. Consequently, the VSM switches conduct only a fraction of the load current in this topology. This represents a significant advantage in terms of conduction losses and improved semiconductor utilization when compared to the FCC. In the FCC, the FCC switches conduct the full load current, i.e. $I_{s,\text{rms}} = I_o$. This is a major benefit of the proposed topology.

TABLE II
MAIN CIRCUIT PARAMETERS

Symbol	Parameter	Value
V_H	Input Voltage	1000 V
V_o	Output Voltage	145 V
P_o	Output Power	3.7 kW
f_{ac}	Fundamental AC Frequency	50 kHz
f_{sw}	VSM Switching Frequency	25 kHz
N	Number of VSMs	4
V_c	Nominal VSM Capacitor Voltage	330 V
C	VSM Capacitor Capacitance	5 µF
L_1	CWS HF5712-561M-25AH	557 µH
L_2	4 x E71/33/32-3C92	221 µH
C_o	Output Capacitor	160 µF
C_i	Input Capacitor	160 µF
$S_{u,i}, S_{l,i}$	SiC MOSFET, C3M0032120K VSM Dead-Time	- 200ns
D_1, D_2	SiC Schottky Diode, MSC50DC70HJ	-

VIII. EXPERIMENTAL RESULTS

In this section, experimental results are presented for the proposed topology covering both steady-state and transient operating conditions. Additionally, efficiency results are provided along with a breakdown of the losses at a representative operating point.

One example of an application for the converter is to interface a dc household to a MVDC distribution line (for instance, 3kVdc to 400 Vdc). To validate the topology for similar applications, a laboratory-scale converter system was designed and experimentally tested. The main circuit parameters for the 1000–145 Vdc, 3.7 kW experimental system are given in Table II. A picture of the experimental prototype is provided in Fig. 7. The number of VSMs is $N = 4$, the switching frequency of each VSM is $f_{\text{sw}} = 25$kHz and the effective ac frequency is $f_{\text{ac}} = 50$kHz. Each VSM capacitor has a capacitance of 5μF and an average voltage of 330 V. The controller is implemented via a PLECS RT Box.

A. Steady-State Experimental Results

The steady-state experimental results are provided in Fig. 8. For these results, the input and output voltages are 1000 and 145 Vdc, respectively. This represents a conversion ratio of 6.9:1. In Fig. 8(a), waveforms are provided for the voltage across the input terminals of the CSM, v_t, the two inductor currents, i_{L2} and i_{L1}, and the string current i_s. In Fig. 8(b), waveforms

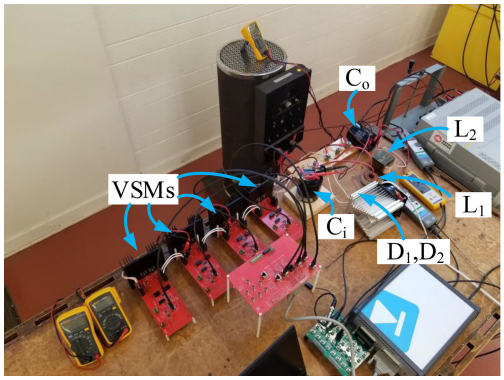

Fig. 7. 1000/145V, 3.7 kW, and 4 VSM experimental prototype.

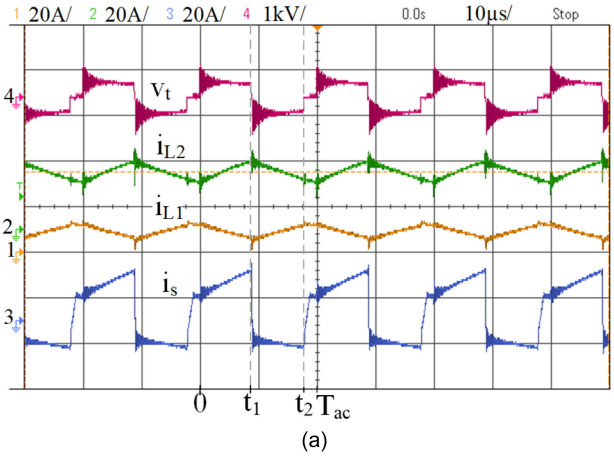

Fig. 8. Steady-state experimental results for 1000 to 145 V. The load current is $I_o = 25.1$ A.

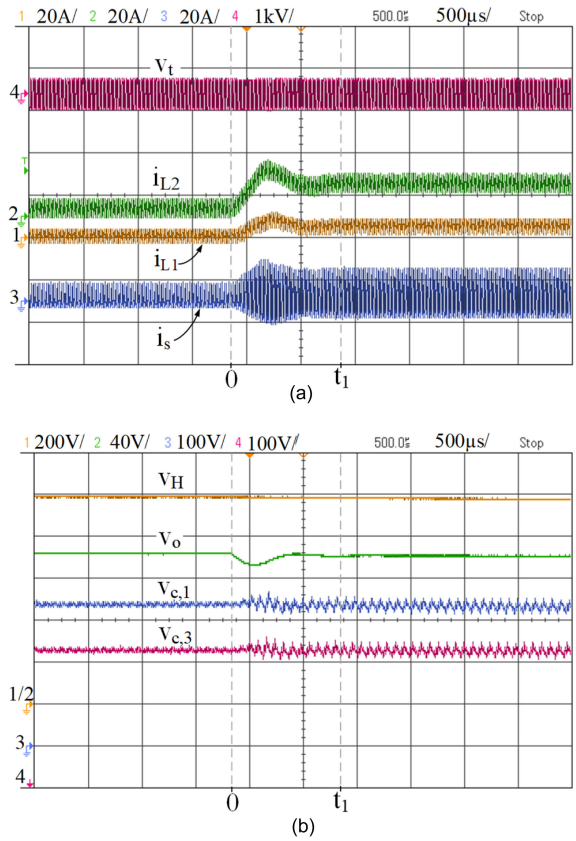

Fig. 9. Transient experimental results for a load step from 10% to 50%.

are provided for the input and output voltages, v_H and v_o, and two representative cell capacitor voltages, $v_{c,1}$ and $v_{c,3}$. The output voltage is shown to be regulated at 145 V. The average CSM inductor currents are approximately $I_{L2} = 25.1$ A and $I_{L1} = 9.5$ A. As can be observed, the two representative cell capacitor voltages are well balanced with average voltages of 330 V each. The peak-to-peak voltage ripple on the cell capacitors is approximately 66 V or 20%. This ripple is somewhat higher than that predicted by (26) due to the available controller hardware requiring slight resequencing of the state machine. The cell capacitor voltage waveforms are nearly identical, and phase displaced by 2 fundamental ac periods. The voltage at the CSM input v_t is shown to have three distinct levels ≈+330V, ≈-330 V and ≈0 V. Each voltage level corresponds to 1 of the 3 states depicted in Fig. 3.

First, state 1 of Fig. 3(a) occurs from $t = 0$ to t_1. During this interval, $v_t \approx 330$ V and the inductor i_{L2} current increases, the inductor i_{L1} current decreases, and the string current is equal to $i_s = i_{L2} - i_{L1}$. Second, state 2 of Fig. 3(b) occurs from $t = t_1$ to $t = t_2$. During this interval, $v_t \approx -330$ V and the inductor i_{L2} current decreases, i_{L1} increases, and the string current is equal to $i_s = -i_{L1}$. Third, state 3 of Fig. 3(c) occurs from $t = t_2$ to $t = T_{ac}$. During this interval, v_t is near zero. In state 3, negligible power is delivered to the CSM inductors as observed in the i_{L1} and i_{L2} current waveforms. The string current is clamped to a maximum value of $i_{L2} - i_{L1}$ in state 3.

It also can be observed that the string current is only a fraction of the output current. The rms value of the string current is approximately $I_{s,\mathrm{rms}} = 12.9$ A. Therefore, the current conducted by the VSM switches is only 51% of the 25.1 A output current. This is less than the maximum bound of 56% obtained from (28). Note, in the FCC, the current conducted by the cell switches would be 25.1 A and therefore the 51% result represents a significant advantage.

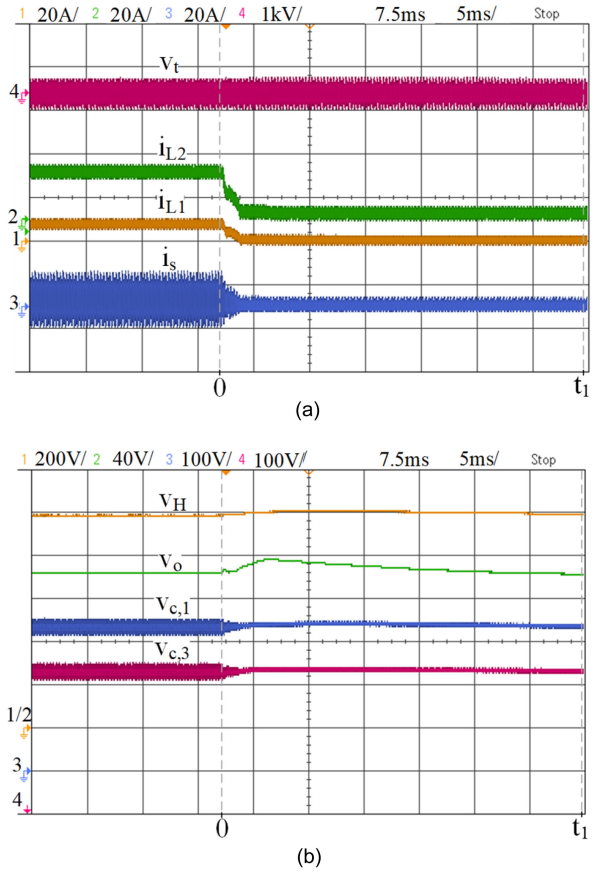

Fig. 10. Transient results for a 90% to 10% partial load rejection.

The effective frequency of the inductor L_1 and L_2 current ripple can be observed to be 50 kHz.

B. Transient Experimental Results

In Fig. 9, a load increase from 3 to 12.6 A is imposed at $t = 0$. It takes approximately 1ms for the system to recover. The string current, i_s, and the inductor currents i_{L1} and i_{L2} are shown to naturally increase in response to the load step. The input voltage and the voltage across the input terminals of the CSM are steady throughout the step change. The voltage ripple on the VSM capacitors is shown to increase in near proportion to the increase in the string current. The output voltage drops from 145 to 133 V before recovering during the step change which represents a voltage dip of 8.3%.

Fig. 10 presents the results of a partial load rejection from 90% to 10% of the rated load. As can be observed, the inductor currents settle within 2 ms. It takes the output voltage approximately 32.5 ms to settle back at the reference voltage of 145 V. The longer settling time in this load rejection case is due to the use of diode switches in the CSM stage which prevents the inductor L_2 current from becoming negative. The output voltage rises to 158 V which represents a voltage swell of 9.7%. The cell capacitor voltage ripple is also shown to decrease because of the reduced string current i_s as expected.

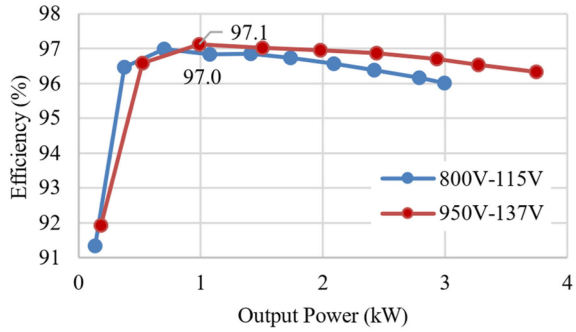

Fig. 11. Efficiency versus Power for 950–137 V and 800–115 V. Peak efficiency is 97.1% at 950 V for 949 W.

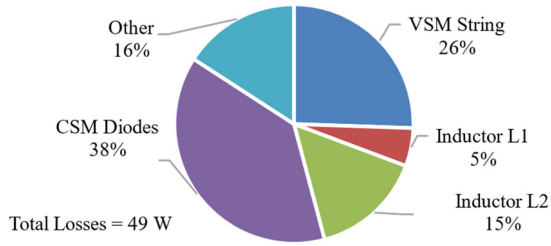

Fig. 12. Measured loss breakdown for 800–115 V at 1.44 kW. Total loss =49W.

C. Efficiency and Losses

Efficiency results are provided in Fig. 11 for two cases: 800 to 115 V and 950 to 137 V. An efficiency at precisely 1000 V was not supported by the available power analyzer. The output power is ramped up to 3 kW for $V_o =$ 115 V and to 3.7 kW for $V_o =$ 137 V to respect component current ratings. The peak efficiency of the converter is 97.1% for 950 to 137 V. For the 950 V case, the efficiency is relatively flat from 1 to 3 kW. A detailed breakdown of the losses by component is provided in Fig. 12 for 800 to 115 V at 1.44 kW operating point. In this loss breakdown, there are disproportionate losses in the CSM diodes due to the relatively low output voltage. Since SiC Schottky diodes were employed, the diode loss is predominately due to the forward voltage drop. The efficiency penalty due to the forward drop of the CSM diodes can be calculated as follows:

$$n_D = (1 - V_d/V_o) * 100\% \tag{29}$$

where V_d represents the forward voltage of one CSM diode. The efficiency penalty due to the CSM diodes will decrease as the output voltage increases and therefore further gains in efficiency can be expected for practical applications.

IX. Conclusion

In this article, a new modular multilevel dc–dc converter with high-power density properties was proposed. The envisioned application for the CS-M2FC is for MVDC applications requiring moderate to high conversion ratios and moderate amounts of power including auxiliary loads for electric trains, dc households, and EVs.

Through the hybrid use of VSMs and a CSM the proposed modular converter was demonstrated to achieve high effective frequencies enabling a commensurate reduction in the cell capacitor sizes. The novel CSM stage as well as the operational approach proposed in this article affords this novel CS-M2FC with advantages including a near 50% reduction in string current and common grounding between the input and output. Additionally, through the proposed operational approach, self-balancing of the VSM capacitor voltages and the ability to regulate a continuous range of output voltages was achieved.

Finally, the proposed converter was verified to be efficient featuring a peak efficiency of 97.1% at an effective frequency of 50 kHz.

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Philippe A. Gray (Student Member, IEEE) received the B.A.Sc. (Hons.) degree in engineering science and the M.A.Sc. degree in electrical engineering in 2010 and 2013, respectively, from the University of Toronto, Toronto, ON, Canada, where he is currently working toward the Ph.D. degree in electrical engineering.

From 2012 to 2013, he was a Visiting Researcher with ABB Corporate Research, Västerås, Sweden. From 2014 to 2017, he was a System Design Engineer of high-voltage dc (HVDC) transmission systems with General Electric, Stafford, U.K. His current research interests include technologies for medium-voltage dc and HVDC applications, multilevel converters, and grid integration of distributed resources.

Peter W. Lehn (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Manitoba, Winnipeg, MN, Canada, in 1990 and 1992, respectively, and the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, Canada, in 1999.

In 1999, he was with the Faculty of the University of Toronto. In 2005, he was a Visiting Professor with the University of Erlangen–Nuremberg, Erlangen, Germany. His current research interests include HVDC technologies, grid integration of storage and renewables, power electronics for electric vehicles, and theoretical analysis of power electronic systems.

Dr. Lehn was an Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION from 2013 to 2019.

Netan Yakop (Student Member, IEEE) received the B.A.Sc. and M.A.Sc. degrees in electrical engineering in 2018 and 2021, respectively, from the University of Toronto, Toronto, ON, Canada.

His research interests include the design and control of multilevel converters and grid integration of distributed generation and energy storage.